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Στην παρούσα εργαστηριακή άσκηση θα μελετηθεί ο τρόπος εγκατάστασης, η υλοποίηση της κατάλληλης συνδεσμολογίας και η λειτουργία της διάταξης Διηλεκτρικής Φασματοσκοπίας *Novocontrol Alpha Analyzer*.

Παρατίθενται παρακάτω οδηγίες και τεχνικά χαρακτηριστικά απο το εγχειρίδιο χρήσης της διάταξης.

Alpha-A High Resolution Dielectric, Conductivity, Impedance and Gain Phase Modular Measurement System

USER's Manual

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1. Safety Precautions

The following safety precautions should be read carefully before using this product.

Before switching the instrument on :

- Ensure that the line power voltage indicated on the Alpha analyzer rear matches the actual voltage of your power line.
Caution : Operating the Alpha analyzer at incorrect line voltage may result in permanent device damage, possibly voiding warranty.
- Ensure that the line power cord is connected only to a power line with protective earth contact. Grounding of any Alpha analyzer parts must not be broken.
Warning : The Alpha power cord contains a separate ground wire for only use with grounded power line outlets. When proper connections are made, the instrument chassis will be connected to the power ground line by the power cord ground wire. Failure of this connection may result in personal injury or death due to electric shock.
- Establish all cable connections as described in the "Setting up the Alpha Analyzer for Measurement" chapter.
- Do not exceed the maximum voltage or current limits specified in the "Instrument Description" chapter for any connectors and sockets.
Caution : Exceeding the specified limits may result in permanent device failure.
- There are no parts inside the Alpha analyzer which require maintenance or adjustments. Therefore the instrument should not be opened. In any case remove the power cord and any test cables before opening the case or removing any parts from the case.
Warning : Opening of the case or removing parts may expose conductors at high lethal voltages if the Alpha analyzer is connected to the power supply.
- To clean the instrument, use a damp cloth or mild water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill the instrument.

2. Inspection

The Alpha analyzer and the test interfaces were tested and mechanically inspected before shipment. After unpacking, inspect all items for obvious physical damage. Report any damage to Novocontrol Technologies immediately. Save the original packing for proving damage that may have occurred during the transit.

The Alpha analyzer is available in several versions. This manual describes only the Alpha-A version. The version letter is labelled as a part of the serial number at the mainframe rear (e. g. letter **A** in 1.0_200_40_50_ANB_01012000). In addition, it is shown in the display in the version field (e. g. letter **A** in V4.1**A**) after switching on or reset. The **N** and **B** letters specify additional mainframe options. Refer to the "Alpha Mainframe, Types and Options" chapter for details.

This Alpha-A analyzer builds a modular measurement system consisting of the Alpha analyzer mainframe and several additional test interfaces.

The **Alpha Mainframe** includes

- Alpha-A analyzer mainframe
- Line power cable
- 3 * BNC cables 100 cm
- Sub-D test interface connection cable 25 pin
- Alpha Analyzer user's manual on cd rom

The following test interfaces may be combined with the mainframe.

The **Active Sample Cell ZGS** includes

- Active sample cell ZGS
- 100Ω calibration standard for active cell
- 2 * active cell test samples with reference measurements as described in the "Performance Test and Frequent Problems" chapter.

The **4-Wire Impedance Interface ZG4** includes

- 4-Wire Impedance Interface ZG4
- Four wire BNC Short calibration standard
- Four wire BNC 100Ω calibration standard
- 4 * BNC cables 25 cm
- 2 * BNC-T adapters
- BNC test sample with reference measurements as described in the "Performance Test and Frequent Problems" chapter.

The **2-Wire Impedance Interface ZG2** includes

- 2-Wire Impedance Interface ZG2
- BNC Short, 100Ω calibration standard
- 2 * BNC cables 25 cm

- BNC test sample with reference measurements as described in the "Performance Test and Frequent Problems" chapter.

The

Potentiostat Galvanostat Electrochemical Interfaces POT/GAL 30V 2A and 15V 10A
High Voltage Interfaces HVB300, HVB1000 and HVB4000
2 Differential Channels High Input Gain Phase Interface G22

test interfaces are described in separate manuals.

3. Introduction

The Alpha Analyzer measures the complex dielectric, conductivity and impedance function of materials in dependence of frequency with high precision. It is especially optimized for dielectric materials with high impedance and low loss factors over a broad frequency range, but can accurately measure high conductive material with low impedance, too.

In addition, if used as a frequency response analyzer in gain phase mode high precision measurement of two ac voltages and their phase relation is supported.

The Alpha analyzer is realized as a modular measurement system with one base unit called the **Alpha analyzer mainframe** and several **test interfaces** which can be connected to the mainframe. Usually the mainframe is supplied with at least one additional test interface. Additional test interfaces may be added later to an existing mainframe.

The Alpha Analyzer Mainframe

provides the basic functionality in order to operate all test interfaces. The mainframe contains a frequency response analyzer with a sine wave and dc-bias generator and two ac voltage input channels.

Each input channel measures the ac voltage amplitude of an applied sine wave. In addition, the phase shift between the sine waves applied to the both inputs is detected. More detailed, each channel measures the amplitude and phase angle of the harmonic base wave component of a signal applied to the input. The harmonic base wave component is measured at the frequency of the ac sine wave generator. Most other signal components are suppressed. In addition, higher harmonics may be measured. Refer to the chapter "Principles of Operation, Frequency Response Analyzer" for details.

Further, the mainframe contains the power supplies, analog and digital control lines and the firmware for operation of the test interfaces.

The following test interfaces can be combined with the mainframe.

Test interfaces for dielectric, conductivity, impedance and gain phase measurements

Active Sample Cell ZGS

Includes an sample cell with two parallel electrode configuration for dielectric, conductivity and impedance measurements on materials. The range and accuracy specifications apply at the

electrodes, cable and cell effects are minimised. The active cell design provides best accuracy and ranges for two electrode material measurements in terms at low loss, high frequency and high impedance performance. The cell can be temperature controlled by one of the Novocontrol temperature control systems between -160 .. 500 °C. In addition 2 channel gain phase measurements are supported.

Ranges: Frequency 3 μ Hz .. 20 MHz, Impedance 0.01 .. 10^{14} Ω , Capacity 1 fF .. 1F, loss factor $\tan(\delta)$ 10^{-5} .. 10^4 , Ac voltage 100 μ V .. 3Vrms, DC Bias -40 .. +40V, 70 mA.

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta) < 3 \cdot 10^{-5}$, absolute phase angle < 2 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase angle < 0.6 m $^\circ$.

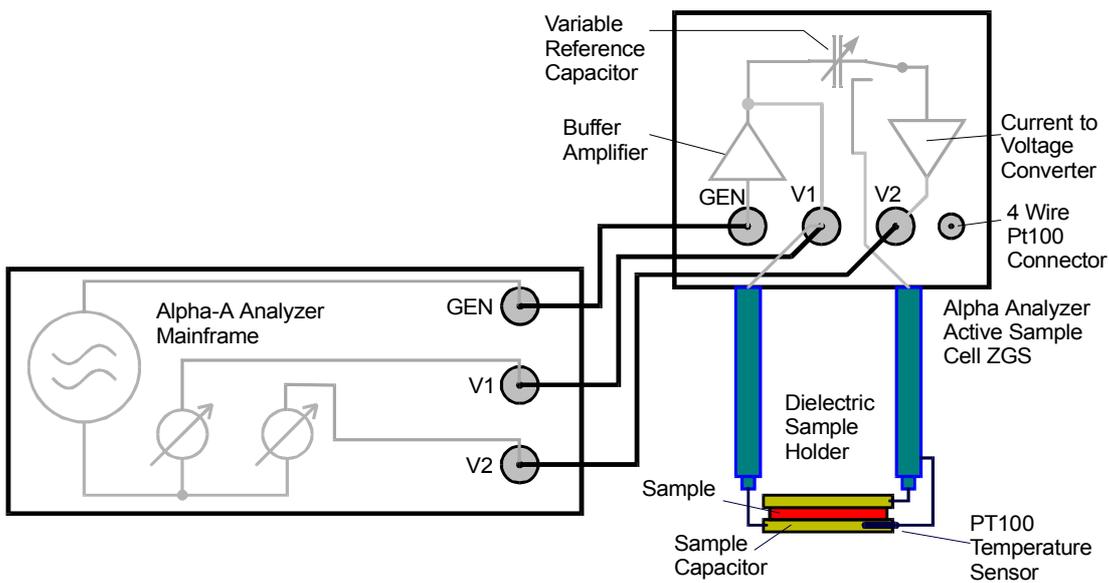


Fig. 1. Setup of an electric material measurement with the active sample cell interface.

4-Wire Impedance Interface ZG4

Includes a test interface for 2-, 3-, and 4-wire dielectric, conductivity, impedance and gain phase measurements. No sample cell is included. Provides measurements with driven shielded high impedance voltage inputs. ZG4 can be used with own sample cells for material measurements. The design allows to locate the external interface close to the sample in order to minimise cable effects. In 2 wire mode, ZG4 can be used with the Novocontrol passive BDS 1200 sample cell.

Ranges: Frequency 3 μ Hz .. 20 MHz, Impedance 0.01 .. 10^{14} Ω , Capacity 1 fF .. 1F, loss factor $\tan(\delta)$ 10^{-5} .. 10^4 , Ac voltage 100 μ V .. 3Vrms, DC Bias -40 .. +40V, 70 mA.

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta) < 3 \cdot 10^{-5}$, absolute phase angle < 2 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase angle < 0.6 m $^\circ$.

Impedance differential voltage inputs: 10^{12} Ω | 10 pF

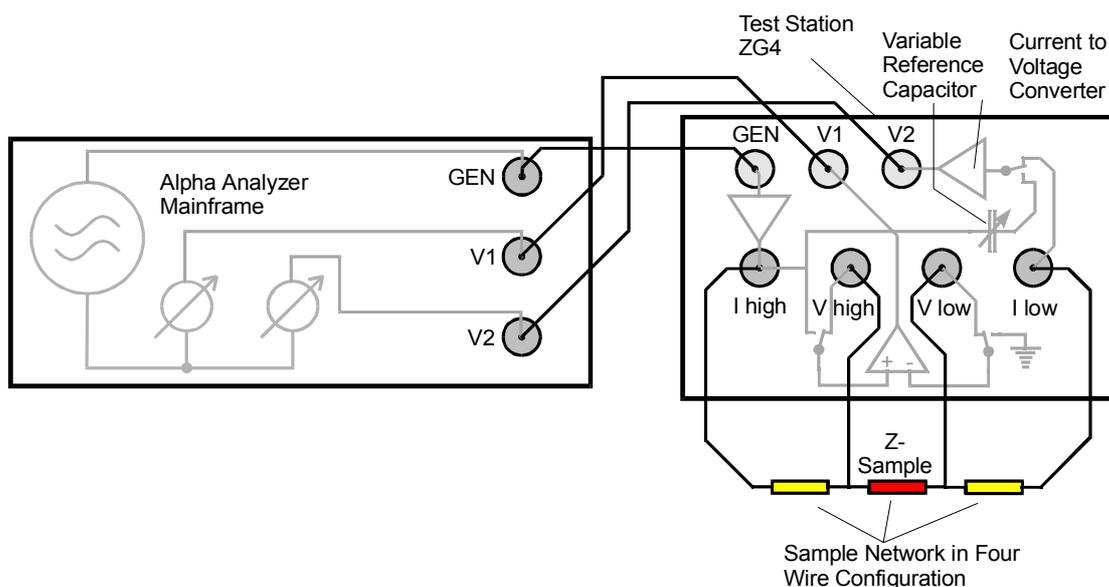


Fig. 2. Setup of an electric measurement with the **ZG4** interface for a 4-wire measurement with differential inputs V high and V low.

2-Wire Impedance Interface ZG2

This is an economical version of the ZG4 interface but restricted to 2-wire dielectric, conductivity, impedance and gain phase measurements. It can be used with the Novocontrol passive BDS 1200 cell or own 2-wire sample cells.

Ranges: Frequency 3 μHz .. 20 MHz, Impedance 0.01 .. 10^{14} Ω , Capacity 1 fF .. 1F, loss factor $\tan(\delta)$ 10^{-5} .. 10^4 , Ac voltage 100 μV .. 3Vrms, DC Bias -40 .. +40V, 70 mA.

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta) < 3 \cdot 10^{-5}$, absolute phase angle < 2 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase angle < 0.6 m $^\circ$.

Potentiostat Galvanostat Electrochemical Interface POT/GAL 30V 2A

Includes a test interface for 2-, 3-, and 4-wire dielectric, conductivity, impedance and gain phase measurements with controlled superimposed dc voltage (Potentiostat) or current (Galvanostat). No sample cell is included. Provides measurements with driven shielded high impedance voltage inputs. POT/GAL can be used with own sample cells for material measurements and is especially suited for electrochemical samples which require controlled dc cell parameters or higher sample currents.

Ranges: Frequency 3 μHz .. 1 MHz, Impedance 0.001 .. 10^{13} Ω , Capacity 10 fF .. 1F, loss factor $\tan(\delta)$ 10^{-4} .. 10^4 , Ac output voltage 20 μV .. 21Vrms, DC Bias -30V .. +30V, 2A.

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta) < 10^{-4}$, absolute phase angle < 6 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase < 0.6 m $^\circ$.

Impedance differential voltage inputs: 10^{12} Ω | 10 pF

Potentiostat Galvanostat Electrochemical Interface POT/GAL 15V 10A

Is similar to POT/GAL 30V 2A but with different output voltage and current.

Ranges: Frequency 3 μ Hz .. 1 MHz, Impedance 0.001 .. 10^{13} Ω , Capacity 10 fF .. 1F, loss factor $\tan(\delta)$ 10^{-4} .. 10^4 , Ac output voltage 10 μ V .. 10.6Vrms, DC Bias -15V .. +15V, 10A.

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta)$, $< 10^{-4}$,
absolute phase angle < 6 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase < 0.6 m $^\circ$.

Impedance differential voltage inputs: 10^{12} Ω | 10 pF

Test interfaces for dielectric, conductivity and impedance measurements**High Voltage 300 Vpp Test Interface HVB300**

Includes a test interface for high voltage dielectric, conductivity and impedance measurements with up to 300 Vpp ac and / or dc voltage applied to the sample. It can be used for measurements of materials under stress and for non linear dielectric, conductivity and impedance spectroscopy.

Ranges: Frequency 3 μ Hz .. 1 MHz, Impedance 0.1 .. 10^{15} Ω , Capacity 1 fF .. 0.1F, loss factor $\tan(\delta)$ 10^{-5} .. 10^4 , Ac output voltage 4 mV .. 108Vrms, DC Bias -150V .. +150V, 70 mA, output impedance 200 Ω .

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta)$, $< 3 \cdot 10^{-5}$,
absolute phase angle < 2 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase < 0.6 m $^\circ$.

High Voltage 1000 Vpp Test Interface HVB1000

Is similar to HVB300 but provides ac and / or dc voltages up to 1000 Vpp.

Ranges: Frequency 3 μ Hz .. 10 kHz, Impedance 1 .. 10^{15} Ω , Capacity 1 fF .. 0.1F, loss factor $\tan(\delta)$ 10^{-5} .. 10^4 , Ac output voltage 12 mV .. 355Vrms, DC Bias -500V .. +500V, 3.3 mA, output impedance 150 k Ω .

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta)$, $< 3 \cdot 10^{-5}$,
absolute phase angle < 2 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase < 0.6 m $^\circ$.

High Voltage 4000 Vpp Test Interface HVB4000

Is similar to HVB1000 but provides ac and / or dc voltages up to 4000 Vpp.

Ranges: Frequency 3 μ Hz .. 10 kHz, Impedance 10 .. 10^{15} Ω , Capacity 1 fF .. 0.1F, loss factor $\tan(\delta)$ 10^{-5} .. 10^4 , Ac output voltage 48 mV .. 1418Vrms, DC Bias -2000V .. +2000V, 2.7 mA, output impedance 750 k Ω .

Accuracy: Relative impedance or capacity, absolute loss factor $\tan(\delta)$, $< 3 \cdot 10^{-5}$,
absolute phase angle < 2 m $^\circ$.

Resolution: loss factor $\tan(\delta)$, impedance, capacity $< 10^{-5}$, phase < 0.6 m $^\circ$.

Test interfaces for gain phase measurements

2 Differential Channels High Input Gain Phase Interface G22

For high accuracy gain phase measurements. Provides 2 voltage channels for gain phase measurements. Each channel has high impedance differential inputs with driven shields for cable capacity elimination.

Ranges: Frequency 3 μ Hz .. 20 MHz, Ac output voltage 0.1 mV .. 3Vrms, DC Bias -40V .. +40V, 70 mA.

Accuracy: $V1 / V2 < 3 \cdot 10^{-4}$, phase angle < 10 m $^\circ$.

Resolution: $V1 / V2 < 10^{-5}$, phase angle < 0.6 m $^\circ$.

Impedance differential voltage inputs: $10^{12} \Omega$ | 10 pF

4. Principle of Dielectric, Conductivity and Impedance Measurement

The principle of a electric material measurement is shown below.

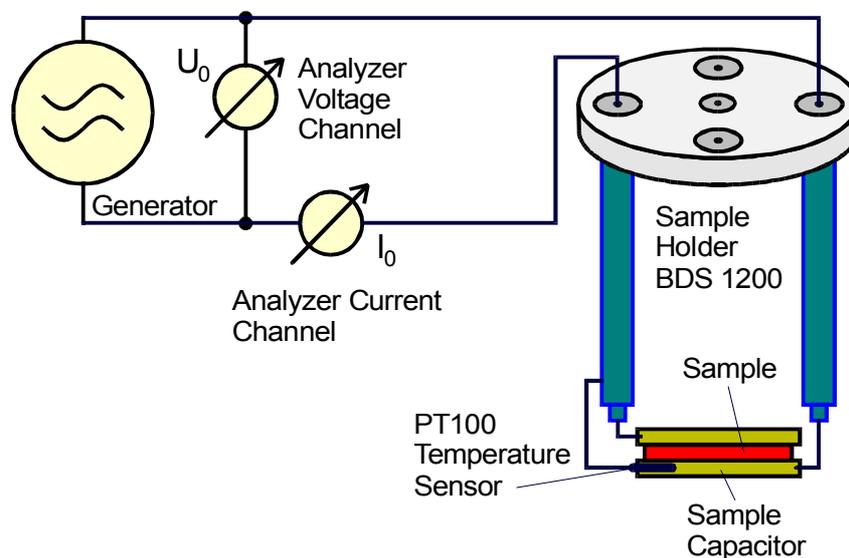


Fig. 3. Principle of a dielectric or impedance measurement.

The sample material is usually mounted in a sample cell between two electrodes forming a sample capacitor. For details, refer to the "Sample Preparation and Measurement Accuracy" chapter.

A voltage U_0 with a fixed frequency $\omega/2\pi$ is applied to the sample capacitor. U_0 causes a current I_0 at the same frequency in the sample. In addition, there will generally be a phase shift between current and voltage described by the phase angle φ .

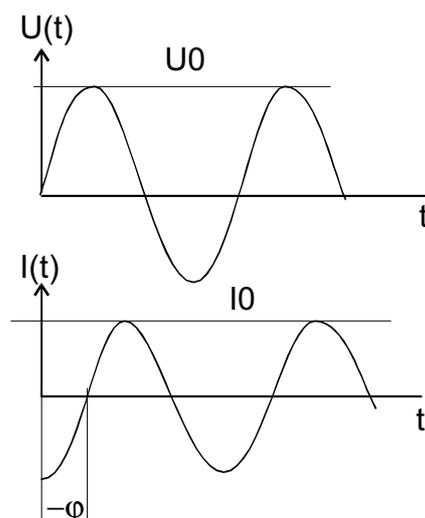


Fig. 4. Amplitude and phase relations between voltage and current of a sample capacitor for electric measurements.

The ratio between U_0 and I_0 and the phase angle φ are determined by the sample material electric properties (permittivity and conductivity) and the sample geometry. For easy calculation and representation of the formulas, it is convenient to use complex notation.

$$U(t) = U_0 \cos(\omega t) = \operatorname{Re}(U^* \exp(i\omega t))$$

$$I(t) = I_0 \cos(\omega t + \varphi) = \operatorname{Re}(I^* \exp(i\omega t))$$

with

$$U^* = U_0$$

and

$$I^* = I' + iI''; \quad I_0 = \sqrt{I'^2 + I''^2}; \quad \tan(\varphi) = \frac{I''}{I'}$$

For a sample with linear electromagnetic response, the measured impedance of the sample capacitor

$$Z^* = Z' + iZ'' = \frac{U^*}{I^*} \quad (1)$$

is connected with the dielectric function of the sample material by

$$\varepsilon^*(\omega) = \varepsilon' - i\varepsilon'' = \frac{-i}{\omega Z^*(\omega)} \frac{1}{C_0} \quad (2)$$

where C_0 is the capacity of the empty sample capacitor.

The specific conductivity σ^* is related to the dielectric function by

$$\sigma^* = \sigma' - i\sigma'' = i2\pi f \varepsilon_0 (\varepsilon^* - 1)$$

5. Principle of Gain Phase Measurement

As described in the previous chapter, in impedance mode the response voltage and current of a sample to an applied sine wave signal are measured.

In gain phase mode, a second voltage is measured instead of the current. This allows to measure two response voltages of an applied sine wave driver signal at two arbitrary points of a system under test (SUT). The two voltages are measured with the Alpha frequency response analyzer (FRA) channels CH1 and CH2. The applied sine wave is created by the Alpha sine wave generator.

A typical application would e. g. be to measure the transfer function of an amplifier or transformer. In this case, the Alpha generator output and input CH1 have to be connected to amplifier input and the Alpha input CH2 to the amplifier output. The amplifier complex transfer function defined by V_{out}/V_{in} is determined by measuring the voltages at CH2 and CH1 and dividing them.

It should be noted, that in gain phase mode the Alpha can be used like a digital lock in amplifier with two input channels, too. The main function of a lock in amplifier is to apply a signal with a defined frequency to a system under test and to measure a response signal. As a further lock in amplifier feature, only the frequency component of the applied signal in the response signal is detected. As usually most of the response signals noise and dc errors are at other frequencies, they will therefore be suppressed. The Alpha uses the same principle, but has in addition a second voltage channel and better accuracy as most lock in amplifiers. For details, refer to the chapter "Principles of Operation, Frequency Response Analyzer".

6. Special Alpha Analyzer Features

If the setup in fig. 3 of the previous chapter is used for measuring electric material properties, the following problems may arise.

Wide Impedance Range

Most dielectric samples have low conductivity ($\epsilon'' \ll \epsilon'$) and behave in a first order approximation as a capacitor. Therefore, the impedance Z of these samples at low frequencies generally becomes very high (e.g. $10^{14} \Omega$ at 0.01 Hz). On the other hand, as the impedance of a capacitor decreases with $1/\text{frequency}$, the sample impedance is generally low at the high frequency end (e.g. 10Ω at 10 MHz). In addition, if the sample has conductivity, it may have low impedance (e.g. 1Ω) over the entire frequency range. Therefore, the current channel of the setup in fig. 3 has to be operated over an extreme wide range (e.g. from 10^{-14} A .. 0.1 A).

This feature is implemented in the Alpha test interfaces for impedance measurement which most of can measure impedance from 0.01Ω .. $10^{14} \Omega$ allowing to measure dielectric samples down to lowest frequencies in the μHz range.

The wide impedance range results in an exceptional capacity range too, which is from 1 fF (0.001 pF) .. 1 F.

This is in contrast to (so called) general impedance analyzers typically covering an impedance range from 0.01Ω .. $10^8 \Omega$. For these analyzers, the high impedance limit ($10^8 \Omega$) confines the measurement of dielectric samples to frequencies of typically $> 10 \text{ Hz}$.

Low Loss Capability

Many dielectric samples have very low loss factors $\tan(\delta)=\epsilon''/\epsilon'$ down to 10^{-4} or even 10^{-5} . $\tan(\delta)$ is determined by the phase angle φ of the measured voltage to the measured current (see. fig. 4). Therefore, if $\tan(\delta)$ is very small, the absolute value of the phase angle φ has to be measured with very high precision (e.g. for $\tan(\delta) = 10^{-5}$, δ and $\varphi=90^\circ-\delta$ have to be measured with a absolute precision of 0.001°).

This can be done by most of the Alpha test interfaces for impedance measurement due to the following two features.

First the Alpha mainframe frequency response analyzer part works with a digitally design optimized for high phase and amplitude resolution.

Second, remaining phase deviations due to analog components in the signal path like amplifiers or the current to voltage converter are cancelled out by a special reference technique used in the test interfaces for impedance measurements. Refer to the "Principle of Operation, Reference Measurement" chapter for details.

This is in contrast to general impedance analyzers which typically have a phase angle accuracy of 0.1° .. 1° corresponding to a $\tan(\delta)$ limit of 10^{-3} .. 10^{-2} .

Cable and Cell Effects Minimised, Accuracy Specified at the Electrodes or Close to the Sample

For frequencies > 1 MHz, the sample impedance may become in the same order as the inductive impedance of the BNC cables connecting the sample holder with the analyzer. This limits the measurement to frequencies below approximately 3 MHz. For high impedance samples, long cables cause additional problems due to electrical noise created by mechanical vibrations. Therefore, the cable length should be kept as short as possible for optimum high frequency and high impedance performance.

This is realized for the active sample cell **ZGS** as shown in fig. 1. The sensitive part of the input amplifiers are directly incorporated on top of the dielectric sample cell or in the active interface. The connection to the sample cell is done which customized air insulated lines optimized both for high frequency performance and isolation at high impedance. This setup can measure electric material samples (with not too low loss factors) up to 20 MHz. A similar concept is realized for the other external interfaces as shown e.g. in fig. 2 for the **ZG4** interface. As the interface is separated from the mainframe it can be located close to the sample and sample connections cables can be kept short.

Contact and Interface Layer Effects Excluded

For some samples it is difficult to apply proper electrodes. In this case, the electrode - sample contact impedance may contribute an unknown error to the measurement. E. g. for an ion conductor with metal electrodes, ions may accumulate at the electrode surface and create an interface polarization layer. The influence of the contact impedance can be reduced, if two additional contacts are applied to the sample in order measure the sample potential separately from the sample current. This technique can be used in order to characterise the interface polarization layers, too.

For this purpose, the **ZG4** and **POT/GAL** interfaces include an additional differential input amplifier with two high impedance voltage inputs which can be used in order to cancel out contact or interface layer impedance. For details refer to the "Principles of Operation, 3- and 4-Wire Impedance Measurement" chapter.

Controlled Cell Potential and Current for Electrolytes and Electrochemical Cells

Measurements of electrolytes or electrochemical cells often require a defined dc potential (Potentiostat) or current (Galvanostat) applied to the sample which is superimposed to the ac signal for impedance measurement. In addition, these applications require often higher sample currents and voltages. These requirements are met by the **Electrochemical Interfaces POT/GAL**. In contrast to other electrochemical equipment, which is often limited in accuracy and impedance range, the **POT/GAL** interfaces have comparable accuracy and impedance range as the other Alpha test interfaces.

Non Linear and Stress Measurements at High Voltage

With the **HVB300**, **HVB1000** and **HVB4000** interfaces, the generator ac voltage and dc bias voltage range can be extended to 300 Vpp, 1000 Vpp or respectively 4000 Vpp. This is useful in order to detect non linear effects in materials and improve the quality of data for high impedance samples at low frequencies. In addition, for many technical materials it is required to measure them at an electrical field similar to the one which they will be exposed in a later applications.

High Measurement Data Point Rate for Monitoring of Fast Time Variant Processes

Usually, the response of gain phase or impedance analyzers is rather slow. Typically data point rates including start of measurement and reading the results by the GPIB port are in the ranges of 10 data points / s for general impedance analyzers and 0.2 data points / s for dielectric measurement systems with reference measurement technique.

As a unique feature, the Alpha analyzer with high speed option **F** supports data point rates up to 157 impedance or 210 gain phase data points per second via the GPIB port. This allows to monitor fast time variant processes with a time resolution down to 5 ms. Refer to the "Data Point Rates" chapter for details.

7. Alpha Mainframe

The Alpha mainframe is the master unit for an modular measurement system for electric frequency domain measurements. Usually the mainframe is operated in combination with one or more additional test interfaces.

The mainframe contains a frequency response analyzer with a sine wave and dc-bias generator and two ac voltage input channels.

In addition, the mainframe contains the power supplies, analog and digital control lines and the firmware for operation of the test interfaces. Refer to the "Introduction" for an overview of the test interfaces available.

After power on, the mainframe automatically detects the connected test interface and adjust the system functionality to it.

Without a test interface, the mainframe can perform gain phase measurements as described in the "Gain Phase Measurements with Alpha Mainframe Only" chapter.

7.1. Types and Options

The Alpha mainframe types and available options are shown below.

Alpha mainframe types	First and second version letter
Upper frequency limit 40 MHz	AT
Upper frequency limit 20 MHz	AN
Upper frequency limit 3 MHz	AK
Upper frequency limit 0.3 MHz	AL

Tab. 1. Alpha mainframe types

Alpha mainframe options	Additional version letters
Dc bias +-40V, 70mA	B if installed, missing else
High measurement speed. Support of measurement rates up to 157 impedance or 210 gain phase data points per second via GPIB port. Refer to the "Data Point Rates" chapter for details.	F if installed, missing else

Tab. 2. Alpha mainframe options

The version letters are contained

- in the serial number at the at the mainframe rear (e.g. ANBF in 4.1_200_40_50_ANBF_01012003 for the 20 MHz version with dc bias and high speed) and
- in the display power up messages described in the next chapter.

Note:

- The upper frequency limit of the mainframe in combination with a test interface is the minimum of either the upper mainframe upper limit or the test interface upper limit.
- If the mainframe does not support the dc bias option, it will be unavailable for all test interfaces too, except for the POT/GAL interfaces which have internal dc bias circuits.

7.2. Front Panel

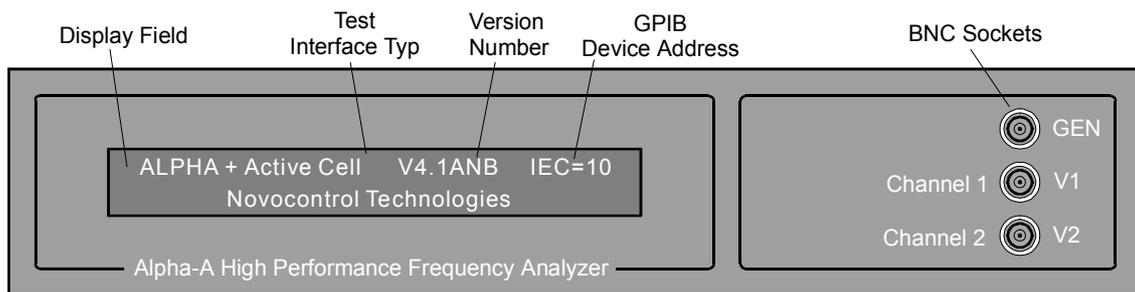


Fig. 5: Alpha mainframe front panel.

The front panel contains the following elements.

The **Display Field** gives information on the actual instrument state depending on the state of operation. Refer to the "Display" chapter for details.

After switching the instrument on, the display shows after about 10 seconds internal boot time its first power up message

"Alpha Dielectric / Impedance Analyzer"
" Novocontrol Technologies".

This first power up message lasts for about 3 seconds and no GPIB commands should be send to the analyzer within this time.

After the first power up message or after a software reset, the second power up message is displayed as shown in fig. 5 and the analyzer is ready for operation. The first display line contains the following elements.

"Alpha" mainframe indicator.

Test Interface Type: The actual detected test interface type.

Instrument version: It is made up by the mainframe firmware number (e.g. **4.1**) and the version letters **"AXY"** for the Alpha-A analyzer mainframe type and options as described in the "Types and Options" chapter.

GPIB Device Address: The actual Alpha GPIB IEEE 488 device address. Refer to the "GPIB IEEE 488 Interface, Alpha GPIB Address" chapter for details.

BNC Sockets

GEN Terminal

Provides an ac output signal for the signal output amplifier mounted in a test interface or acts as the signal source for stand alone gain phase measurements.

If the Alpha mainframe is operated with an test interface, the GEN socket should be connected to the corresponding test interface GEN socket and should only be used for this purpose.

If the Alpha mainframe is used stand alone without a test interface as a gain phase analyzer, the GEN socket should be used as the voltage driver signal source.

The GEN terminal has 50 Ω output impedance and max. 1.36 Vrms voltage amplitude.

Do not apply any external voltage or current to the GEN socket.

V1 Terminal

Voltage input terminal for the frequency response analyzer channel 1.

If the Alpha mainframe is operated with an test interface, the V1 socket should be connected to the corresponding test interface V1 socket and should only be used for this purpose.

If the Alpha mainframe is used stand alone as a gain phase analyzer, the V1 socket should be used as the input for gain phase voltage channel 1.

V2 Terminal

Voltage input terminal for the frequency response analyzer channel 2.

If the Alpha mainframe is operated with an test interface in impedance mode, the V2 socket should be connected to the corresponding test interface V2 socket and should only be used for this purpose.

If the Alpha mainframe is operated with an test interface in gain phase mode or stand alone in gain phase mode, for many but not all test interfaces the V2 socket should be used as the input for gain phase voltage channel 2. For details refer to the " System Setup for Gain Phase Mode" chapters of the test interfaces.

V1 and **V2** have input impedance 1 M Ω in parallel with capacity < 100 pF.

The maximum voltage range of each voltage input can be selected from 9 ranges from 3 Vrms to 0.03 Vrms. Each input can be dc or ac coupled. Refer to the "Principles of Operation, Frequency Response Analyzer" chapter for details.

Voltage limits : Inputs are protected for maximum of +- 45 V dc voltage superimposed by maximum 4 Vrms ac voltage.

7.3. Rear Panel

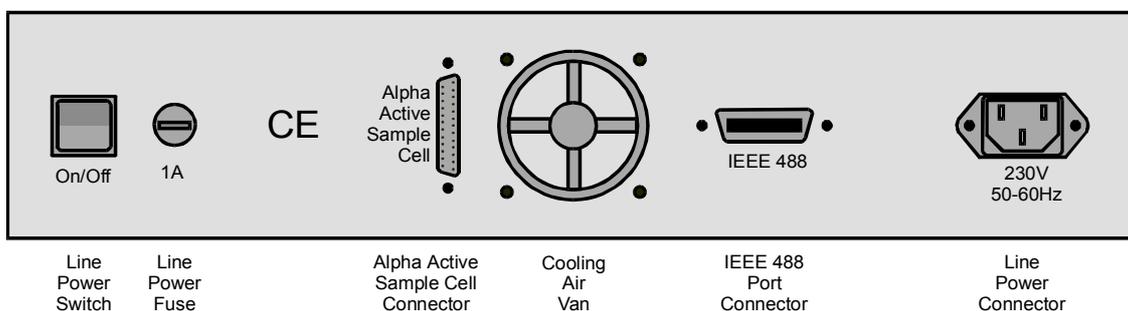


Fig. 6: Rear panel of the Alpha analyzer mainframe.

The rear panel contains the following elements :

Line Power Connector. Follow the procedure below to connect the Alpha analyzer to the line power.

Make sure that the line voltage indicated below the Alpha line connector matches your actual line voltage. There is no option for changing the Alpha analyzer line voltage. If the line voltage does not match your actual line voltage, contact Novocontrol GmbH for replacement by another instrument.

Caution : Operating the Alpha analyzer at incorrect line voltage may result in permanent device damage, possibly voiding warranty.

Do not switch the instrument on before connected to the line power. Do not switch the instrument on before all other connections described in the following sub chapters are done.

Connect the female end of the supplied power supply cord the Alpha **Line Power Connector**. Connect the other end of the power cord to a grounded AC line outlet.

Warning : The Alpha power cord contains a separate ground wire for only use with grounded outlets. When proper connections are made, the instrument chassis is connected to the power ground line by the power cord ground wire. Failure of this connection may result in personal injury or death due to electric shock.

GPIB IEEE 488 Connector. Used in order to connect the Alpha analyzer to the IEEE 488 GPIB controller port of a host computer. This port is also known as IEC or GPIB port. Refer to the "GPIB IEEE 488 Interface" chapter for details.

Cooling Air Van. Provides an air stream from the instrument front to the rear for internal temperature stabilisation. The air inlet is at the bottom plate front side. Make sure that the air inlet is free. At least 1 cm spacing should be allowed for proper air fluctuation. This is especially important if the Alpha is mounted into a 19" rack.

Alpha Active Sample Cell Connector. This connector is used in order to connect a test interface to the Alpha mainframe.

Switch off the Alpha mainframe and the test interface (if it has an own power supply) before connecting or disconnecting the test interface to the mainframe.

Use only the 25 pin Sub-D cable supplied by Novocontrol. The cable provides a one to one connection for each of the 25 pins.

Warning : This connector provides operating power and control voltages for the test interface. Do not connect any other devices to this terminal. Connecting other devices (like serial or parallel ports) may result in damage of devices. Use only the original cable delivered by Novocontrol.

Line Power Fuse. The fuse protects the Alpha power cord. Generally, the fuse should not break except for internal malfunction of the Alpha analyzer. Therefore in case of break, it is recommended to contact Novocontrol GmbH for support. If the fuse has to be replaced:

Switch the instrument off. Disconnect the power cord first from the line power and then from the Alpha **Line Power Connector**.

Replace the fuse by the following types :

1A, slow blow for line voltage 220V-240V

2A, slow blow for line voltage 110V.

Line Power Switch. Switches the Alpha mainframe on and off. Do not switch the instrument on before connected to the line power. Do not switch the instrument on before all other connections described in the following sub chapters are done.

7.4. Gain Phase Measurements with Alpha Mainframe Only

The Alpha mainframe can be operated in gain phase mode as a stand alone frequency response analyzer without a test interface.

In this mode the generator ac output voltage is from 45 μ Vrms .. 1.36 Vrms and dc bias is not available.

The maximum voltage range of each voltage input can be selected from 9 ranges from 3 Vrms to 0.03 Vrms. Each input can be dc or ac coupled. Refer to the "Principles of Operation, Frequency Response Analyzer" chapter for details.

V1 and **V2** have input impedance 1 M Ω in parallel with capacity < 100 pF.

Voltage limits : Inputs are protected for maximum of +- 45 V dc voltage superimposed by maximum 4 Vrms ac voltage.

The measurement setup is shown below.

Caution : Before setting up any connections :

- **Switch off the Alpha analyzer and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**
- **Respect the voltage and current limitations described in the "Alpha Mainframe, Front Panel" chapter.**

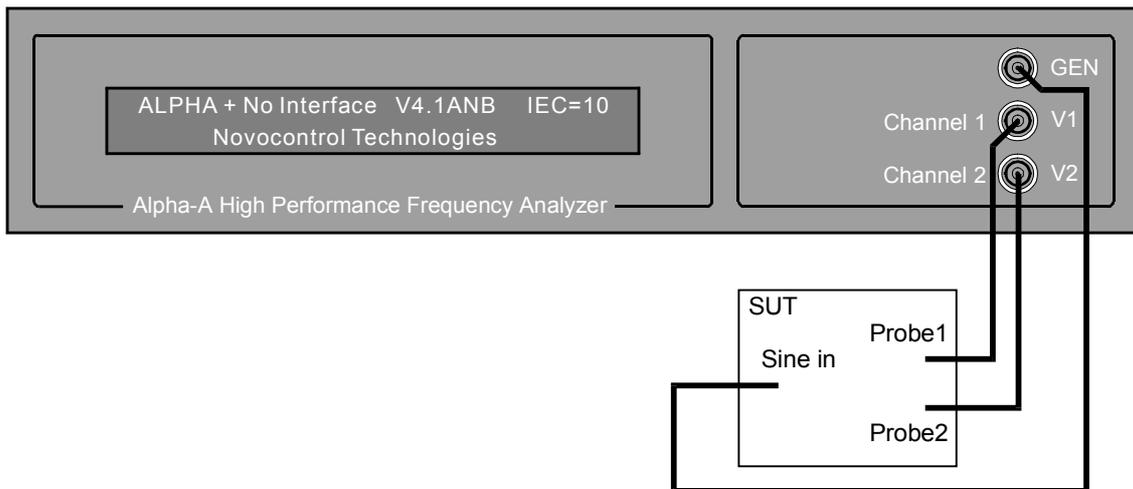


Fig. 7. Connections of the Alpha mainframe without a test interface to a system under test (SUT) in gain phase mode.

Note: If higher input impedance, higher ac signal amplitude, higher sensitivity, dc bias or differential inputs are required, operation with the **2 Differential Channels High Input Gain Phase Interface G22** is recommended.

8. Test Interfaces for Dielectric, Conductivity, Impedance and Gain Phase Measurements

Test interfaces extend the performance of the Alpha analyzer mainframe. An overview on the available test interfaces is given in the "Introduction" chapter.

8.1. Active Sample Cell ZGS

The active sample cell ZGS is optimized for dielectric, conductivity and impedance measurements of materials. It includes a sample cell in which the sample material is mounted between two parallel plate electrodes.

The cell includes all components which are crucial for wide band, wide impedance range and high accurate measurements like output-, input amplifiers, reference capacitors, connection lines, electrode mounting and insulation.

The cell realises a turn key measurement system in the sense that the user has not to care about cable and cell effects. The range and accuracy specifications apply therefore at the electrodes. Due to the active cell design with the critical electronic components in the cell head, cable and cell effects can be minimised.

The active cell design provides best accuracy and ranges for two electrode material measurements in terms at low loss, high frequency and high impedance performance.

The cell can be temperature controlled by on the Novocontrol temperature control systems between -160 .. 500 °C. In addition 2 channel gain phase measurements are supported.

8.1.1. Instrument Description

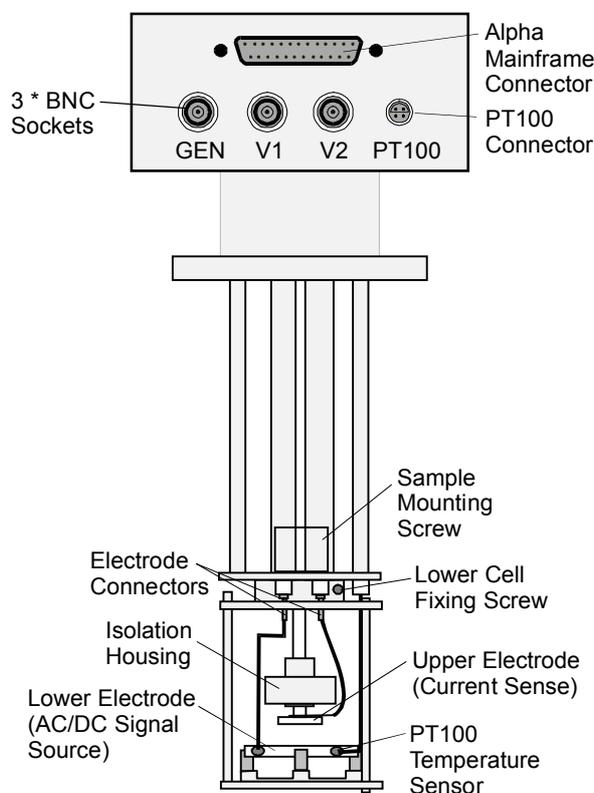


Fig. 8: Active Sample Cell ZGS.

The active sample cell ZGS contains the following elements :

Alpha Mainframe Connector. It should be connected to the **Alpha Active Sample Cell Connector** on the Alpha mainframe rear, providing power and control lines for the active sample cell.

Caution : Do not connect any other devices to this terminal. Connecting other devices (like serial or parallel ports) may result in damage of devices. Use only the original cable supplied by Novocontrol.

GEN Terminal

This is the input socket for the active sample cell voltage buffer amplifier. It should be connected to the **GEN** socket of the Alpha mainframe. This input should not be connected to other terminals. Maximum voltage limit : ± 3 Vrms.

V1 Terminal

In impedance mode, it should be connected to the **V1** socket of the Alpha mainframe for sensing the voltage applied to the sample by the **Upper Electrode**. **V1** is internally connected to the voltage signal generator (buffer amplifier) output and the **Lower Electrode**.

V1 should be used in gain phase mode as the driver signal for the sample system under test.

This output is short protected to system ground. Do not apply any external voltages or currents.

V2 Terminal

Provides the voltage output of the cell internal current to voltage converter. For dielectric or impedance measurements it should be connected to the **V2** socket of the Alpha mainframe.

This output is short protected to system ground. Do not apply any external voltages or currents.

PT100 Connector

This 4 wire connector can be used for sensing the sample temperature. This is done with a PT100 temperature sensor mounted in the **Lower Electrode** plate. The PT100 is connected as shown below.

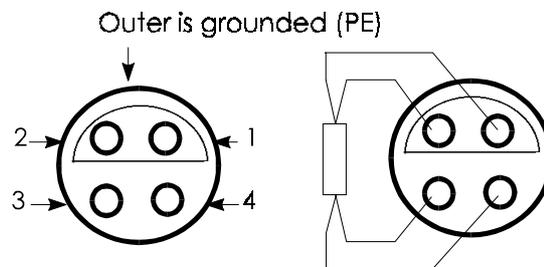


Fig. 9. PT100 temperature connector of the active sample cell.

Upper Electrode

The sample should be mounted between the **Upper** and **Lower Electrode**. For details of sample preparation and mounting refer to the "Sample Preparation and Measurement Accuracy" chapter. The **Upper Electrode** senses the sample current.

Current limits : Protected to ± 200 mA. DC Voltages up to ± 50 V maybe applied as long the current limits are not exceeded.

Lower Electrode

Applies the signal generator output voltage to the sample material. The **Lower Electrode** is internally connected to the **V1** output of the active sample cell. The output voltage is 0 .. 3 Vrms ac superimposed by optional +40 V dc (bias). The output impedance is 50 Ω. The maximum dc bias current is limited to about 70 mA.

This output is short protected to system ground. Do not apply any external voltages or currents.

The active sample cell lower part containing the electrodes can be separated as shown below. This enables easier handling during the sample preparation and allows the active head to be used with various lower samples cells.

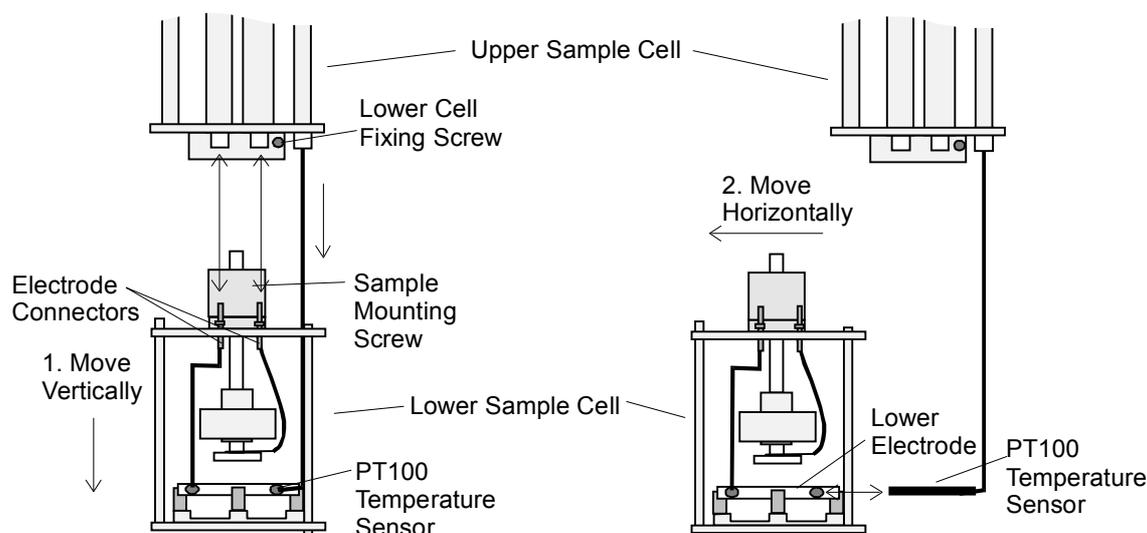


Fig. 10. Procedure of separating the lower sample cell from the upper cell.

In order to separate the **Lower Sample Cell** from the **Upper Sample Cell** :

- Loosen the **Lower Cell Fixing Screw**.
- In a first step, slowly move the lower sample cell vertically to the upper sample cell as shown in fig. 10. While moving stepwise, pull the both **Electrode Connectors** out of the connection lines. The **PT100 Sensor** remains in the lower electrode at this time and shifts itself out of the upper sample cell. The PT100 can be shifted vertically by about 5 cm with respect to the upper sample cell, but can not be disconnected from the upper sample cell.

Warning : Do not pull to strong. Otherwise the PT100 connections maybe damaged.

- In a second step move the lower sample cell horizontally in order pull the PT100 sensor out of the **Lower Electrode**.

Important : If the lower sample cell has to be re-mounted after separation, connect the upper electrode to the thicker line of the active head and the lower electrode to the thinner line. The connections must not be exchanged.

In order to measure a sample, it must be built into the sample capacitor. For this purpose, the sample should not directly be placed between the electrodes of the active sample cell. Instead, it should be placed between two disposable electrodes as shown below. Disposable electrodes are available from Novocontrol GmbH in various diameters.

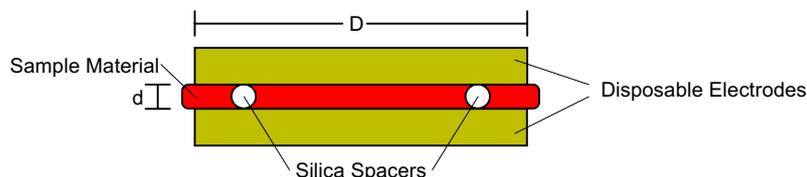


Fig. 11. Sample capacitor prepared with two round disposable plate electrodes.

The two electrodes with the sample between can be seen as a separate sample capacitor which can be placed between the active sample cell electrodes as shown below. This procedure simplifies the sample preparation, protects the electrodes from contamination and allows to remove the sample easily.

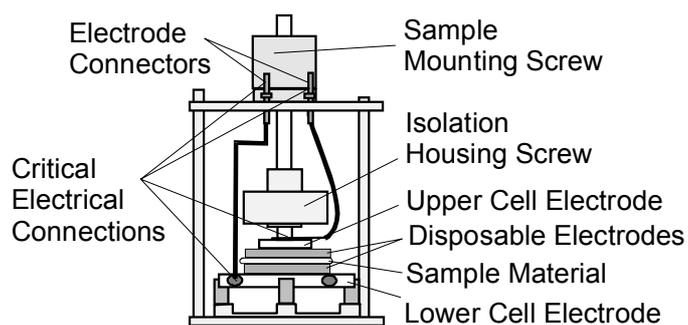


Fig. 12. Lower sample cell part with sample mounted between disposable electrodes.

Important

- Use the **Sample Mounting Screw** in order to fix the **Disposable Electrodes** by the **Upper Cell Electrode**.
Do not use the **Insulation Housing Screw** in order to fix the sample. This may result in improper contact and damage of the upper electrode isolation.
- Before starting a measurement check the **Critical Electrical Connections** for proper contact.
- Tighten to the **Upper Cell Electrode** by rotating it clockwise against the **Isolation Housing Screw** until a fix connection is established.
- Tighten the screw of the **Lower Cell Electrode** connection wire with screw driver until a fix connection is established.

- Check the two **Electrode Connectors** for proper contact with the upper sample cell connection lines.
- From time to time, all four **Critical Electrical Connections** contacts should be cleaned and polished in order to remove insulating oxide layers. This applies especially if the cell was exposed to high temperatures before.

For this purpose :

- remove the **Upper Cell Electrode** by rotating it anti clockwise against the **Isolation Housing Screw**,
- remove the **Lower Cell Electrode** connection wire by unscrewing it from the **Lower Cell Electrode**,
- pull the two electrode connectors out of the upper sample cell connections lines.

For additional sample preparation hints, refer to "Sample Preparation".

8.1.2. System Setup for Impedance Mode

In order to set up the **Active Sample Cell ZGS** for a dielectric, conductivity or impedance measurement, the following connections have to be established.

Caution : Before setting up any connections :

- **Switch off the Alpha mainframe and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**
- **Respect the voltage and current limitations described in the "Instrument Description, Alpha Mainframe Front Panel" chapter.**

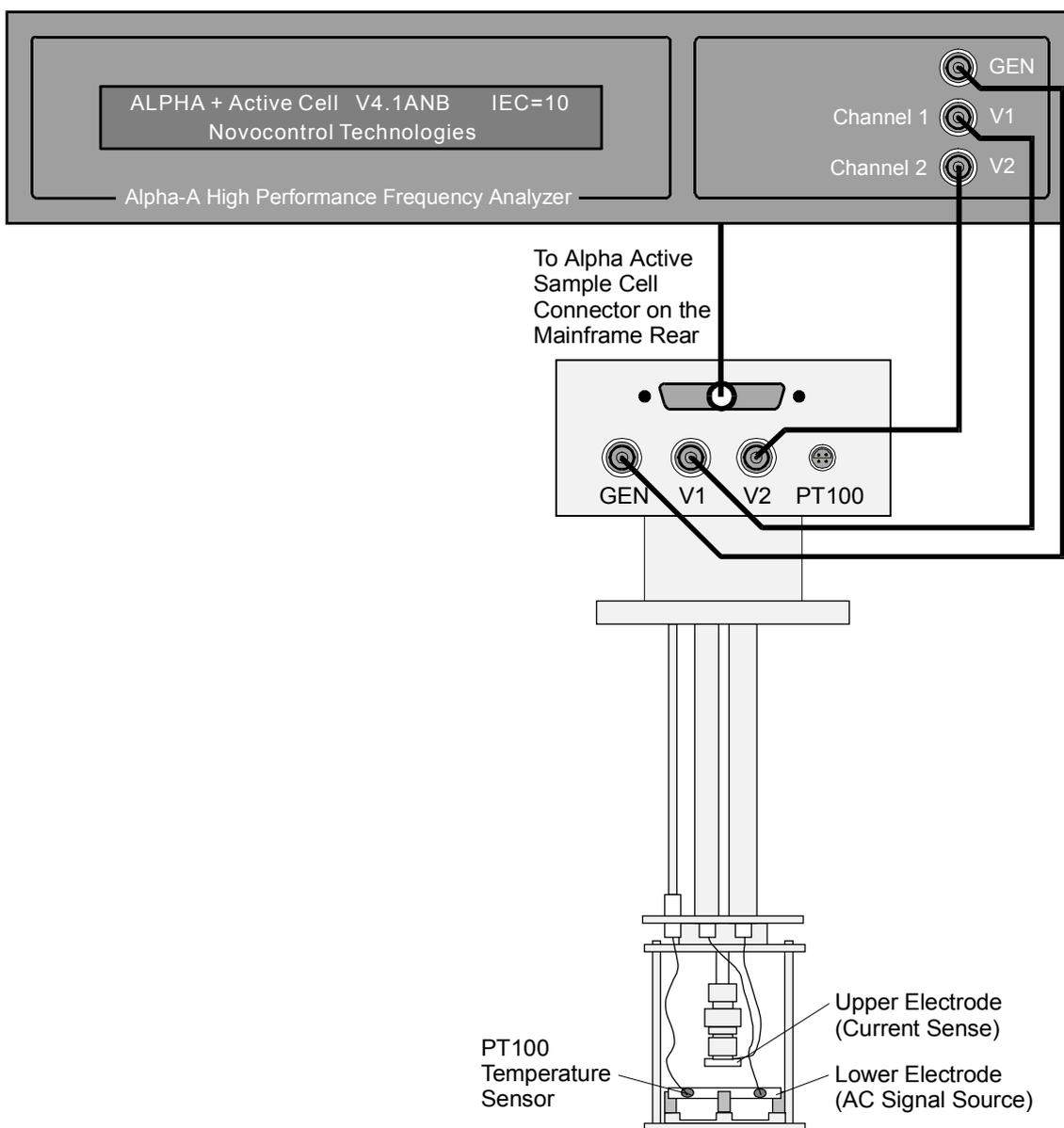


Fig. 13. Connections of the Alpha mainframe with the active sample cell ZGS in impedance mode.

Note : For proper operation, the active sample cell has to be shielded. This is generally done by placing it into a metal cryostat or a metal shielding tube. Both are available from Novocontrol GmbH.

8.1.3. System Setup for Gain Phase Mode

In order to set up the **Active Sample Cell ZGS** for a or gain phase measurement, the following connections are required.

Caution : Before setting up any connections :

- **Switch off the Alpha mainframe and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**
- **Respect the voltage and current limitations described in the "Instrument Description, Alpha Mainframe Front Panel" chapter.**

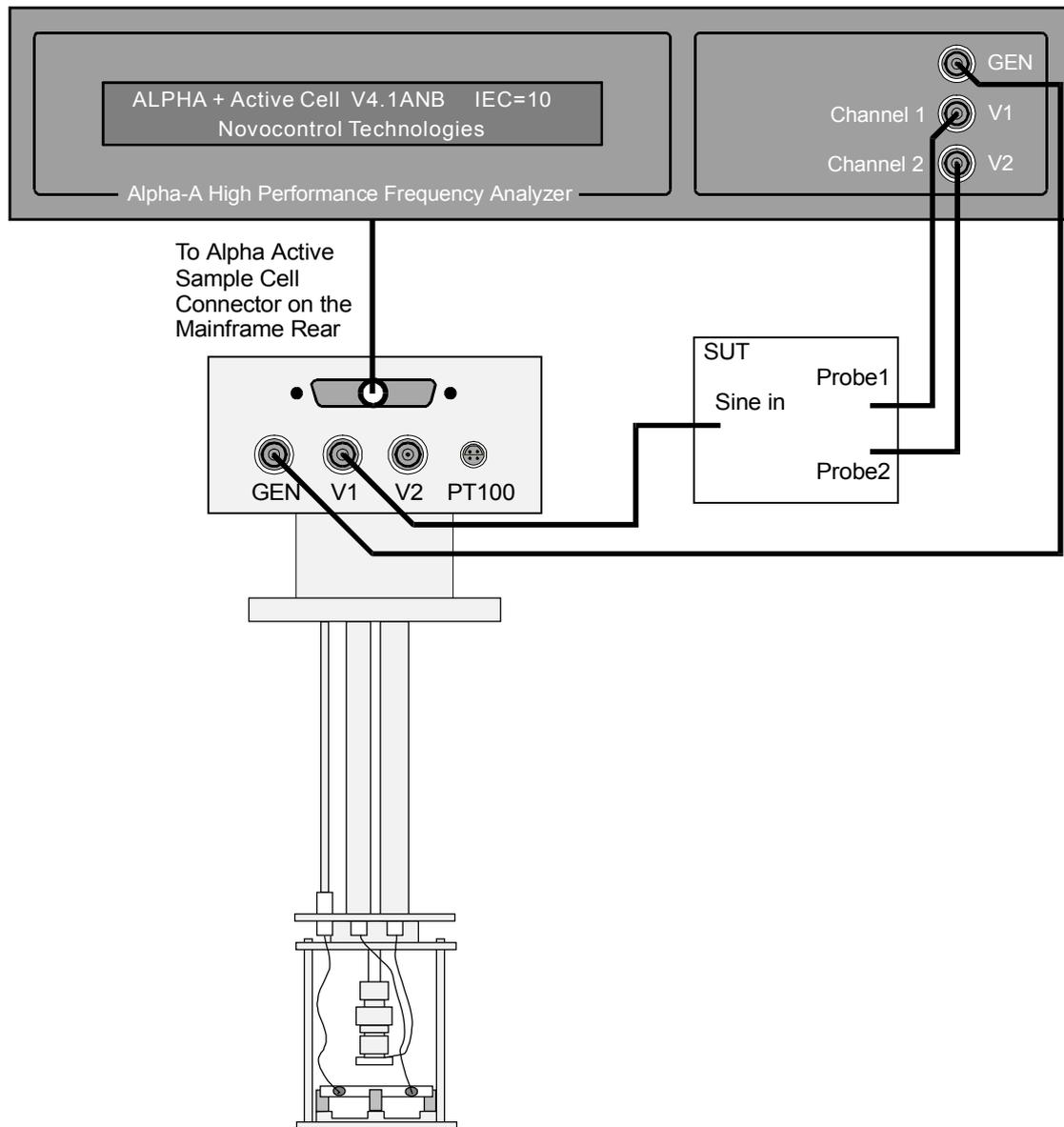


Fig. 14. Connections of the active sample cell to a system under test (SUT) in gain phase mode.

8.2. 4-Wire Impedance Interface ZG4

The 4-wire test interface ZG4 is optimized for 4-, 3-, and 2-wire impedance measurements of components or materials. For dielectric and conductivity material measurements an additional sample cell is required.

The interface contains components which are critical for wide band, wide impedance range and high accurate measurements like output-, differential input amplifiers, current to voltage converter and reference capacitors.

The two additional differential voltage inputs **V high** and **V low** have high impedance ($1\text{ T}\Omega$ | 10 pF) which is necessary for 3- or 4-wire measurements of high impedance samples.

Due to the separate interface design, the interface can be located close to the sample and cable effects can be kept small.

The capacity of the cables to the sample can be further reduced by the driven shield technology. In 2 wire mode, the interface can be used with the Novocontrol passive BDS 1200 sample cell.

In addition, gain phase measurements with one high impedance differential voltage input and one single ended voltage input are supported.

8.2.1. Instrument Description

Front Panel

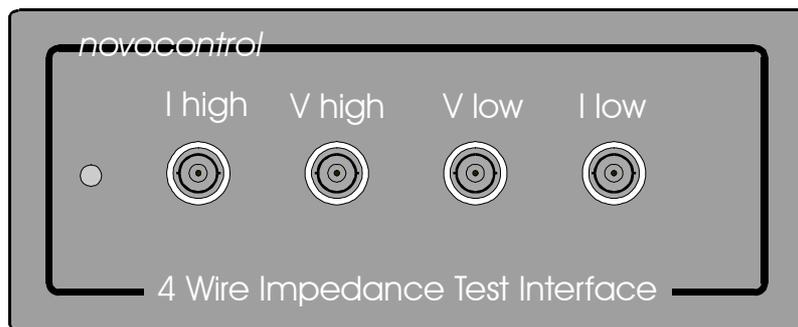


Fig. 15. Interface ZG4 front panel.

It contains the **I high**, **V high**, **V low** and **I low** BNC terminals for sample connection. The usage and connections schemes of these sockets depend on the interface front mode which is impedance or gain phase and 2-, 3-, or 4-wire in both modes. For details refer to the "Setup for Impedance Mode" and "Setup for Gain Phase Mode" chapters. In addition, the outer shields of the **V high** and **V low** terminals can be configured for driven shield operation. Refer to the "Driven Shields" chapter for details.

I high applies the generator signal in order to drive the sample. This applies both in impedance and gain phase mode. The output voltage is between $0 \dots 3\text{ V}_{\text{rms}}$ ac superimposed by optional $\pm 40\text{ V}$ dc (bias). The output impedance is $50\ \Omega$. The maximum dc bias current is limited to about 70 mA . In two wire mode, **I high** is internally connected to the interface differential voltage amplifier positive input.

The ac voltage magnitude, frequency and the optional dc voltage can be adjusted. Refer to the "Principles of Operation, Frequency Response Analyzer" chapter for details.

The **I high** output is protected against shorts to system (earth) ground. Do not apply any external voltage or current.

V high is the interface differential voltage amplifier positive input in three and four wire mode. **V high** is internally not connected in two wire mode.

V low is the interface differential voltage amplifier negative input in four wire mode. **V low** is internally not connected in two or three wire mode.

The maximum voltage range for both voltage **V low**, **V high** inputs can be selected from 9 ranges from 3 Vrms to 0.03 Vrms. Both inputs can be dc or ac coupled. Refer to the "Principles of Operation, Frequency Response Analyzer" chapter for details.

V high and **V low** have input resistance $> 10^{12}\Omega$ in parallel with < 10 pF capacity. The dc bias current at each terminal is $< 2 \cdot 10^{-12}A$.

Voltage limits : Inputs are protected for maximum of ± 45 V dc voltage superimposed by maximum 4 Vrms ac voltage.

I low is the input of the interface current to voltage converter. It should be used in impedance mode in order to sense the response current of a test sample driven by the **I high** socket.

This input is operated at virtual ground, meaning that the voltage at the **I low** is always nearly compensated to 0V by the feedback loop of the internal current amplifier, if the input currents are within the selected range. Therefore, the input impedance is normally (negligible) low against the sample impedance (e.g. 0.1Ω). Anyhow, as the input may be configured for measuring impedance up to $10^{14}\Omega$, in spite of the virtual ground, the input impedance may become quite high (e.g. $10^9\Omega$). Refer to the "Principles of Operation, Current to Voltage Converter" chapter for details.

Current limits : Protected to ± 200 mA. DC Voltages up to ± 50 V maybe applied as long the current limits are not exceeded.

The interface can be configured both in gain phase and in impedance mode for the front modes **2-Wire**, **3-Wire** and **4-Wire**. The front mode is selected either by the Alpha GPIB **FRS=** command or by Novocontrol WinDETA software dialogue Analyzers, Options Alpha, Configuration.

The connections of the differential amplifier inputs with the interface front terminals for the different front modes are shown below.

	2-Wire	3-Wire	4-Wire
V high Terminal	Not connected	Connected to Diff. Amp. +	Connected to Diff. Amp. +
V low Terminal	Not connected	Not connected	Connected to Diff. Amp. -
Diff. Amp. +	Connected to I high	Connected to V high terminal	Connected to V high terminal
Diff. Amp. -	Connected to System Ground	Connected to System Ground	Connected to V low terminal
Ch1 Measures	Voltage at I high	Voltage at V high	Voltage difference V high - V low

Tab. 3. Alpha test interface ZG4 front connections

Diff. Amp. + denotes the interface differential voltage amplifier positive input.

Diff. Amp. - denotes the interface differential voltage amplifier negative input.

Ch1 is the first channel of the Alpha mainframe frequency response analyzer, which receives the signal from the differential amplifier.

Rear Panel

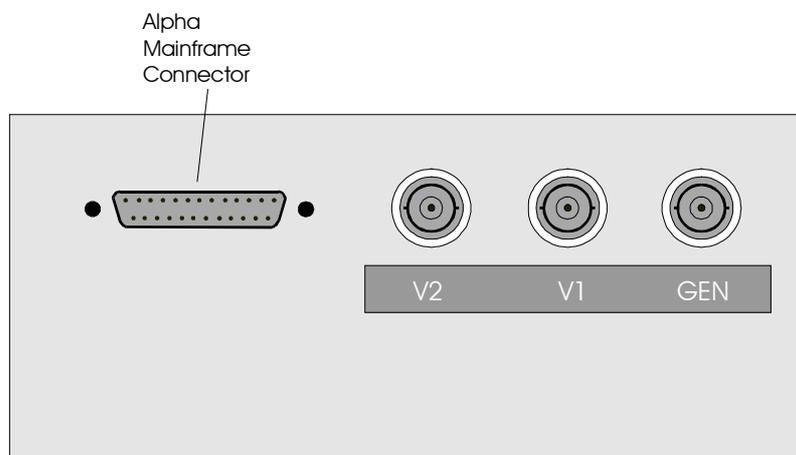


Fig. 16. Interface ZG4 rear panel.

It contains the following elements for connection with the Alpha mainframe.

Alpha Mainframe Connector

It should be connected to the **Alpha Active Sample Cell Connector** on the Alpha mainframe rear, providing power and control lines for the test interface ZG4.

Caution : Do not connect any other devices to this terminal. Connecting other devices (like serial or parallel ports) may result in damage of devices. Use only the original cable delivered by Novocontrol.

GEN Terminal

This is the input socket for the interface driver signal buffer amplifier. It should be connected to the **GEN** socket of the Alpha mainframe. This input should not be connected to other terminals. Maximum voltage limit : +- 3 Vrms.

V1 Terminal

It should always be connected to the **V1** socket of the Alpha mainframe. **V1** is internally connected to the interface differential voltage amplifier output.

Do not short this output to ground. Do not apply any external voltages or currents.

V2 Terminal

Provides the voltage output of the interface current to voltage converter. In impedance mode it should be connected to the **V2** socket of the Alpha mainframe.

This output is short protected to system ground. Do not apply any external voltages or currents.

8.2.2. Setup for Impedance Mode

In order to set up the **Interface ZG4** for impedance measurement, the following connections have to be established.

Caution : Before setting up any connections :

- **Switch off the Alpha analyzer and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**
- **Respect the voltage and current limitations described in the "Instrument Description, Alpha Mainframe Front Panel" chapter.**

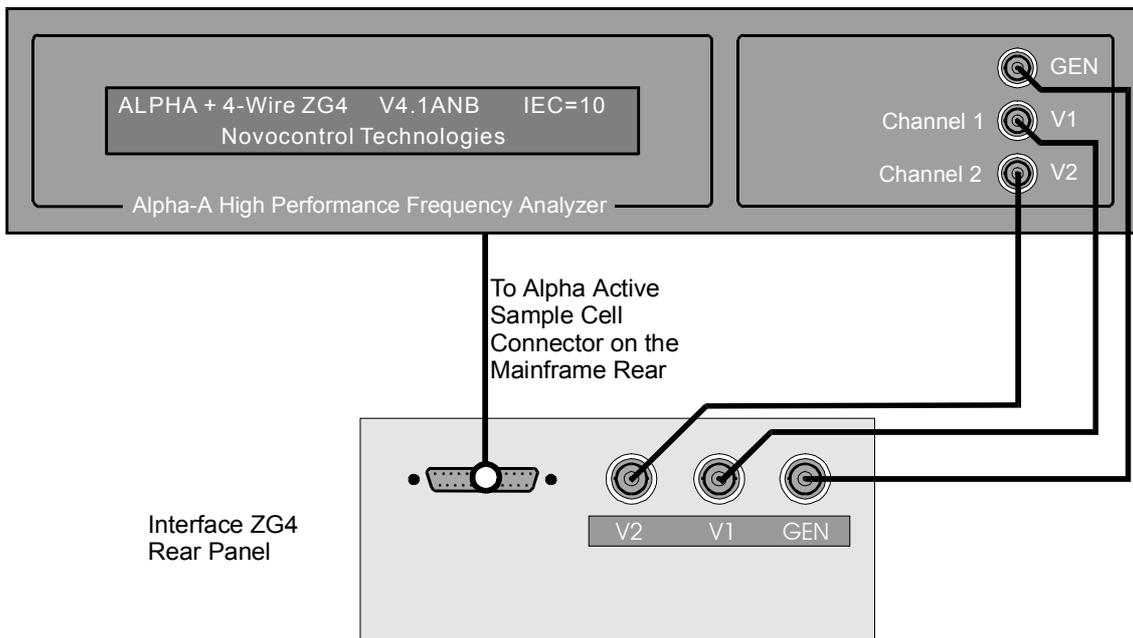


Fig. 17. Connections of the Alpha mainframe and the interface ZG4 rear panel in impedance mode.

Important: For the GEN, V1 and V2 connections use only the 1m BNC cables supplied by Novocontrol. Usage of cables with other wave impedance or length may reduce accuracy.

Depending on the required input configuration which is 2-, 3- or 4 -wire, the following front panel connections should be established.

2-Wire configuration for impedance measurement

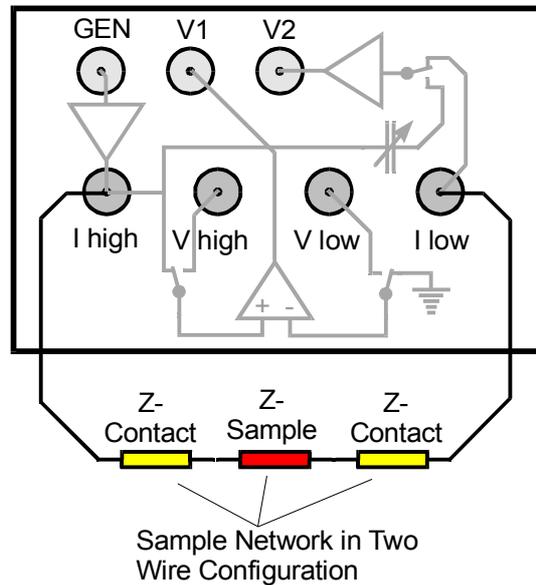


Fig. 18. Interface ZG4 front configuration for 2-wire front mode. For the Novocontrol BDS 1200 sample cell **I high** <-> **Terminal 1** and **I low** <-> **Terminal 4** should be connected.

This is the default and most easy to use mode. Cable and contact impedance are included in the measured impedance. For low impedance samples, the cable impedance may be partly cancelled out by a load short calibration as described in the "Calibrations" chapter.

The two wire configuration mode is selected either by the Alpha **FRS=2** GPIB command or by the WinDETA menu "Analyzers, Options (Alpha), Configuration, 4 Wire Front State, Two Wire".

3-Wire configuration for impedance measurement

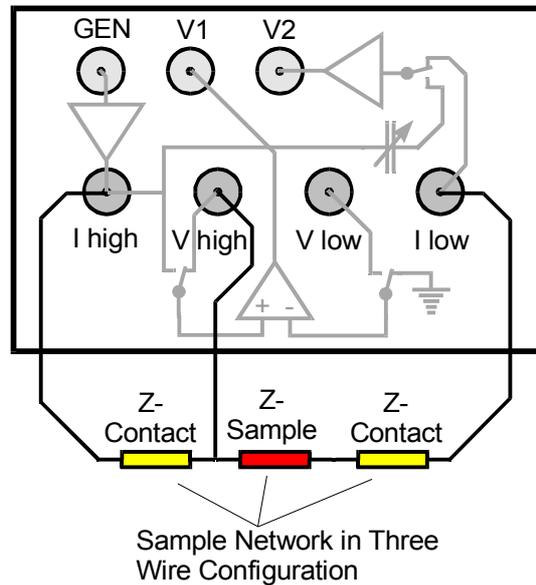


Fig. 19. Interface ZG4 front configuration for 3-wire front mode.

Only the **V high** terminal is used in order to measure the sample voltage at a separate point from the **I high** connection. Cable and contact impedance of the **I low** wire and the corresponding electrode are included in the measured impedance. For low impedance samples, the cable impedance may be partly cancelled out by a load short calibration as described in the "Calibrations" chapter.

If **V high** is attached to the sample by a high impedance contact, make sure that the contact voltage is small against the total measured voltage. For details refer to the "Principles of Operation, Four Wire Impedance Measurement" chapter.

This mode may be used for two wire samples, too. In this case, the **V high** and **I high** cables should be connected at the sample. This will slightly improve high frequency performance compared to the two wire mode with two cables only.

The three wire configuration mode is selected either by the Alpha **FRS=3** GPIB command or by the WinDETA menu "Analyzers, Options (Alpha), Configuration, 4 Wire Front State, Three Wire".

4-Wire configuration for impedance measurement

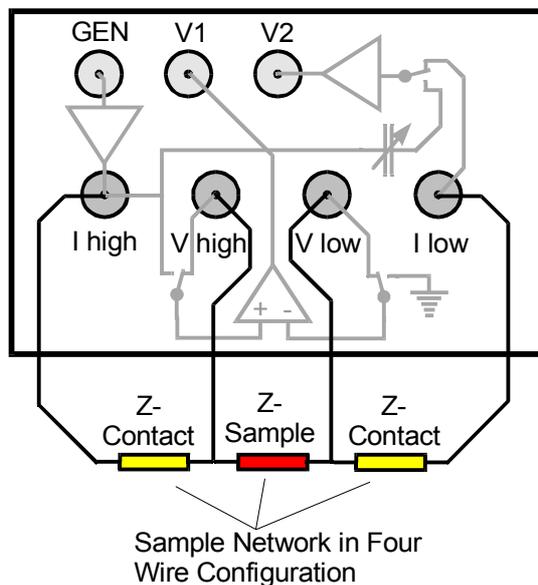


Fig. 20. Interface ZG4 front configuration for 4-wire front mode.

The **V high** and **V low** terminals are used in order to measure the sample voltage at two separate points from the **I high** and **I low** connections. Cable and contact impedance are cancelled out if the current in the **V low** terminal is small against the measured current. If **V high** or **V low** is attached to the sample by a high impedance contact, make sure that the contact voltage is small against the total differential voltage.

Note: In the four wire mode, the **V low** wire may add an additional current to the sample current measured at the **I low** terminal. This may decrease accuracy and usable range for high impedance samples exceeding $10\ \text{T}\Omega$. At higher frequencies, the input and cable capacity at the **V low** terminal may result in an additional error even for samples with lower impedance, too.

Therefore, the four wire mode is only recommended for samples, which can not be easily measured in two or three wire mode. For details refer to the "Principles of Operation, Four Wire Impedance Measurement" chapter.

The four wire configuration mode is selected either by the Alpha **FRS=4** GPIB command or by the WinDETA menu "Analyzers, Options (Alpha), Configuration, 4 Wire Front State, Four Wire".

8.2.3. Setup for Gain Phase Mode

In order to set up the **Interface ZG4** for a or gain phase measurement, the following connections from the Alpha mainframe to the interface are required.

Caution : Before setting up any connections :

- **Switch off the Alpha analyzer and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**

- **Respect the voltage and current limitations described in the "Instrument Description, Alpha Mainframe Front Panel" chapter.**

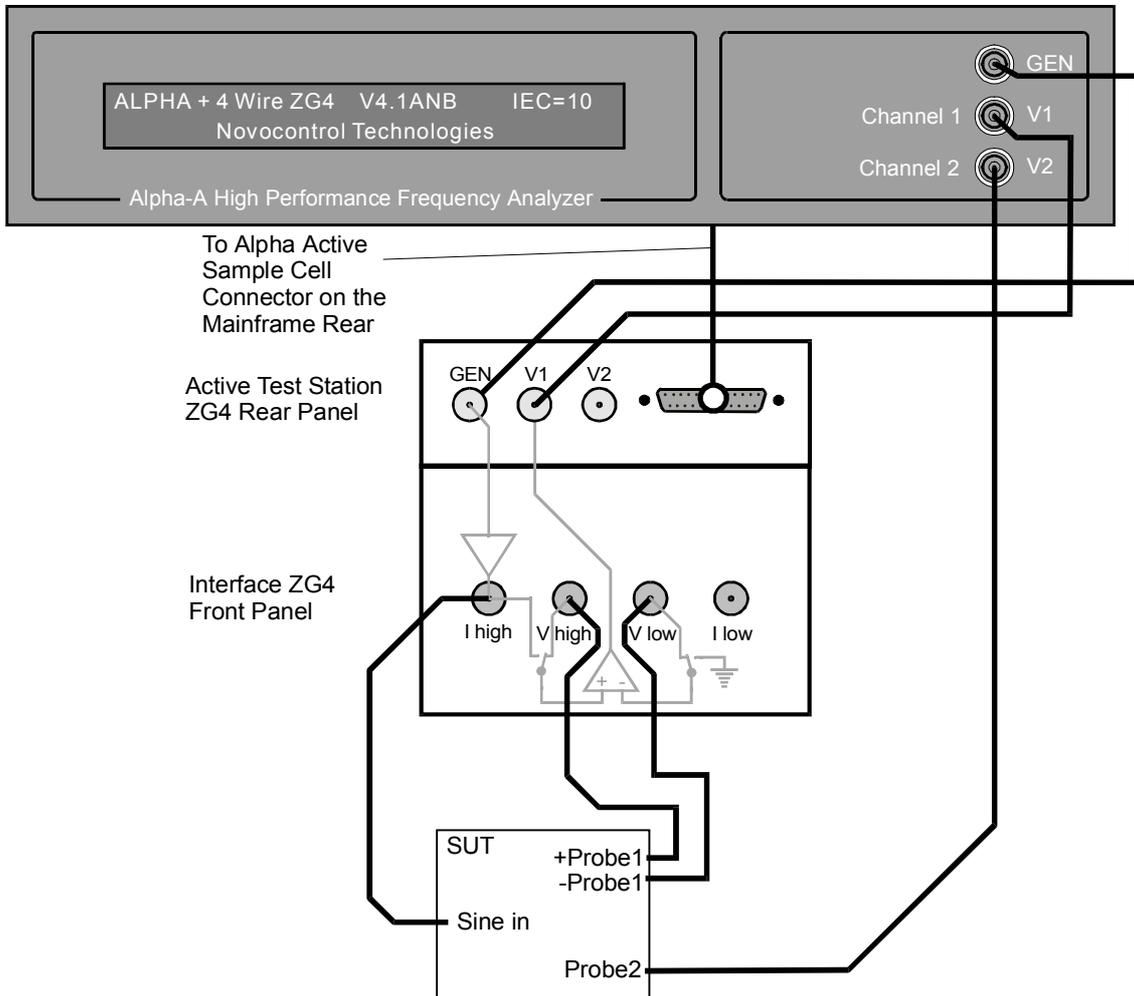


Fig. 21. Interface ZG4 connections to the Alpha main frame in gain phase mode.

Important: For the GEN, V1 and V2 connections use only the 1m BNC cables supplied by Novocontrol. Usage of cables with other wave impedance or length may reduce accuracy.

Fig. 21 shows the configuration in 4-wire front mode. In this mode, the Alpha voltage CH1 measures the difference voltage of the system points +Probe1 and -Probe1. CH2 measures the voltage at Probe2.

In 3-wire front mode, the configuration is similar to fig. 21, but the **V low** terminal and connection is unused. CH1 measures the voltage at point +Probe1.

In 2-wire front mode, the configuration is similar to fig. 21, but the **V high** and **V low** terminals and connections are unused. CH1 measures the voltage at the **I high** terminal.

Note: The **V high** and **V low** terminals have much higher input impedance as the **V2** terminal. Therefore, the **V high** (or **V low**) terminal should be used in order to measure high impedance system points instead of the **V2** terminal.

8.2.4. Driven Shields

The ZG4 interface has two operation modes for the outer shield conductor of the **V high** and **V low** voltage input terminals.

- **Normal mode** with driven shields disabled. The outer BNC terminal conductor is connected to system ground. In this mode, the capacity (about 120 pF / m cable length) of the connection cables from the **V high** and **V low** inputs to the sample adds to the **V high** and **V low** terminals input impedance (about 10 pF | 1 T Ω).
- **Driven shields enabled.** The outer BNC **V high** or **V low** terminal conductor is kept by an internal driven shield amplifier at the same potential as the corresponding inner conductor. This cancels out cable capacity and reduces the input impedance of the inner cable conductor nearly to the terminal input impedance (10 pF | 1 T Ω).

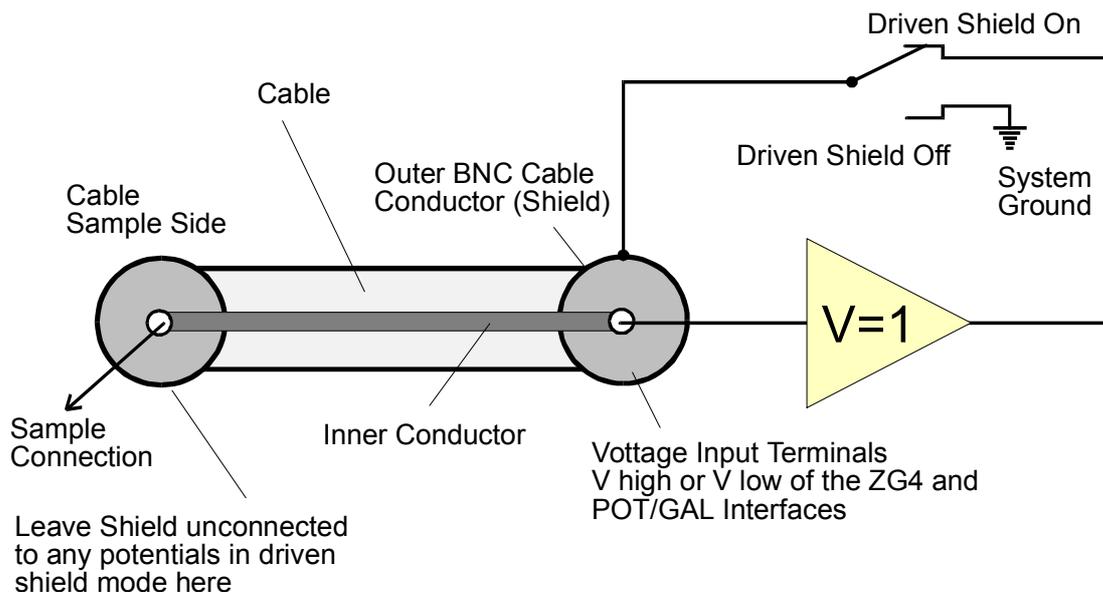


Fig. 22. Interface ZG4 **V high** or **V low** terminal outer shield BNC conductor configuration with driven shield mode enabled.

Note: With driven shield mode enabled:

- The outer BNC conductor of the **V high** or **V low** terminals can be at potentials up to about ± 10 V with respect to system ground. Therefore, the outer shield conductor of the BNC cables should be connected to the outer conductors of the **V high** or **V low** terminals at the interface side but must be left open at the sample side as shown in fig. 22.

- At high frequencies, the **V high** or **V low** cables may radiate electromagnetic fields like an antenna which may interfere with EMV sensitive equipment, broadcasting or communications devices.
- The outer **V high** or **V low** terminal shield conductor is protected to shorts against system ground. **Do not apply any external voltages or currents to the shield.**

The driven shield mode can be activated independent for the **V high** and **V low** terminal by the Alpha **DRS=** GPIB command or from the WinDETA by "Analyzers, Configuration (Alpha Analyzer), Driven Shields".

For details refer to the "Driven Shields Setup for 3- or 4-Wire Impedance Measurements" chapter.

8.3. 2-Wire Impedance Interface ZG2

The 2-wire test interface ZG2 is an economical version of the 4-wire test interface ZG4. It has the same properties as ZG4, except that the differential voltage amplifier is missing and only 2-wire impedance measurements are supported.

ZG2 is optimized for dielectric, conductivity and impedance measurements of components or materials. For material measurements an additional sample cell is required. The Novocontrol BDS 1200 cell is recommended.

The interface includes all components which are critical for wide band, wide impedance range and high accurate measurements like output amplifier, current to voltage converter and reference capacitors.

Due to the separate interface design, the interface can be located close to the sample and cable effects can be kept small.

In addition, gain phase measurements with two single ended voltage inputs are supported.

8.3.1. Instrument Description

Front Panel

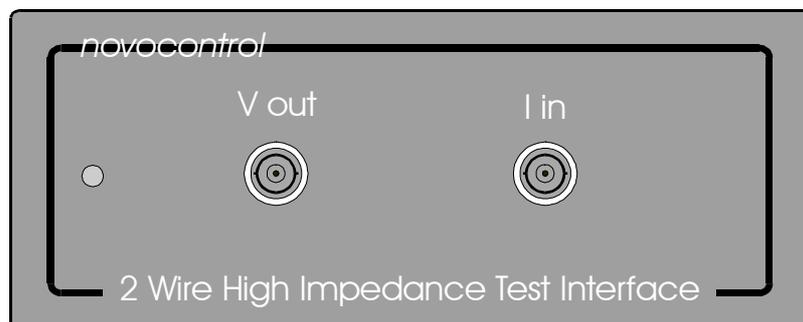


Fig. 23. Interface ZG2 front panel.

It contains the **V out** and **I in** BNC terminals for sample connection. The usage and connections schemes of these sockets depend on the interface front mode which is 2-wire impedance or gain phase. For details refer to the "Setup for Impedance Mode" and "Setup for Gain Phase Mode" chapters.

V out applies the generator signal in order to drive the sample. This applies both in impedance and gain phase mode. The output voltage is between 0 .. 3 Vrms ac superimposed by optional +-40 V dc (bias). The output impedance is 50 Ω . The maximum dc bias current is limited to about 70 mA. **V out** is internally connected to the **V1** rear terminal.

The ac voltage magnitude, frequency and the optional dc voltage can be adjusted. Refer to the "Principles of Operation, Frequency Response Analyzer" chapter for details.

The **V out** output is protected against shorts to system (earth) ground. Do not apply any external voltage or current.

I in is the input of the current to voltage converter. It should be used in impedance mode in order to sense the response current of a test sample driven by the **V out** socket.

This input is operated at virtual ground, meaning that the voltage at **I in** is always nearly compensated to 0V by the feedback loop of the internal current amplifier, if the input currents are within the selected range. Therefore, the input impedance is normally (negligible) low against the sample impedance (e.g. 0.1 Ω). Anyhow, as the input may be configured for measuring impedance up to 10¹⁴ Ω , in spite of the virtual ground, the input impedance may become quite high (e.g. 10⁹ Ω). Refer to the "Principles of Operation, Current to Voltage Converter" chapter for details.

Current limits : Protected to +-200 mA. DC Voltages up to +-50 V maybe applied as long the current limits are not exceeded.

8.3.2. Setup for Impedance Mode

In order to set up the **Interface ZG2** for impedance measurement, the following connections have to be established.

Caution : Before setting up any connections :

- **Switch off the Alpha analyzer and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**
- **Respect the voltage and current limitations described in the "Instrument Description, Alpha Mainframe Front Panel" chapter.**

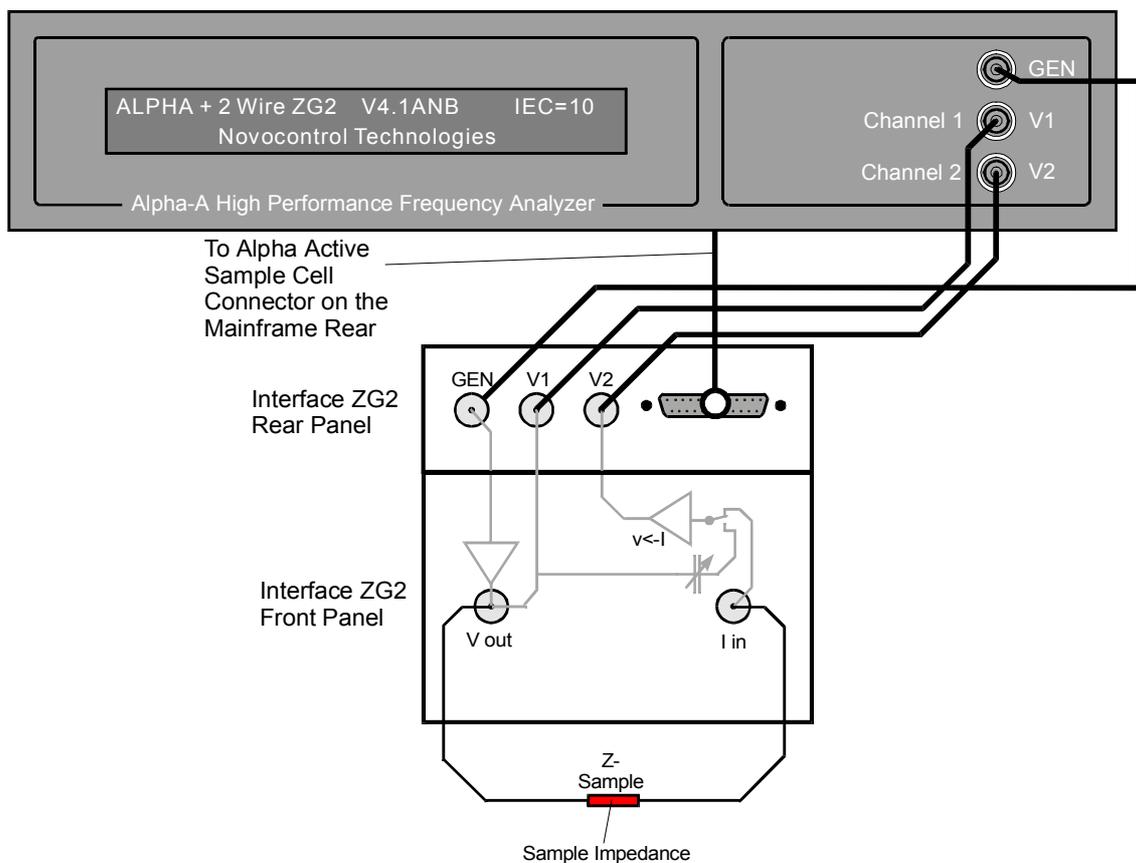


Fig. 24. Connections of the Alpha mainframe and the interface ZG2 in impedance mode.
For the Novocontrol BDS 1200 sample cell **V out** <-> **Terminal 1** and
I in <-> **Terminal 4** should be connected.

Important: For the GEN, V1 and V2 connections use only the 1m BNC cables supplied by Novocontrol. Usage of cables with other wave impedance or length may reduce accuracy.

8.3.3. Setup for Gain Phase Mode

In order to set up the **Interface ZG2** for a gain phase measurement, the following connections from the Alpha mainframe to the interface are required.

Caution : Before setting up any connections :

- **Switch off the Alpha analyzer and all devices connected to it.**
- **Set up all connections as described in the "Rear Panel Connections" chapter.**
- **Respect the voltage and current limitations described in the "Instrument Description, Alpha Mainframe Front Panel" chapter.**

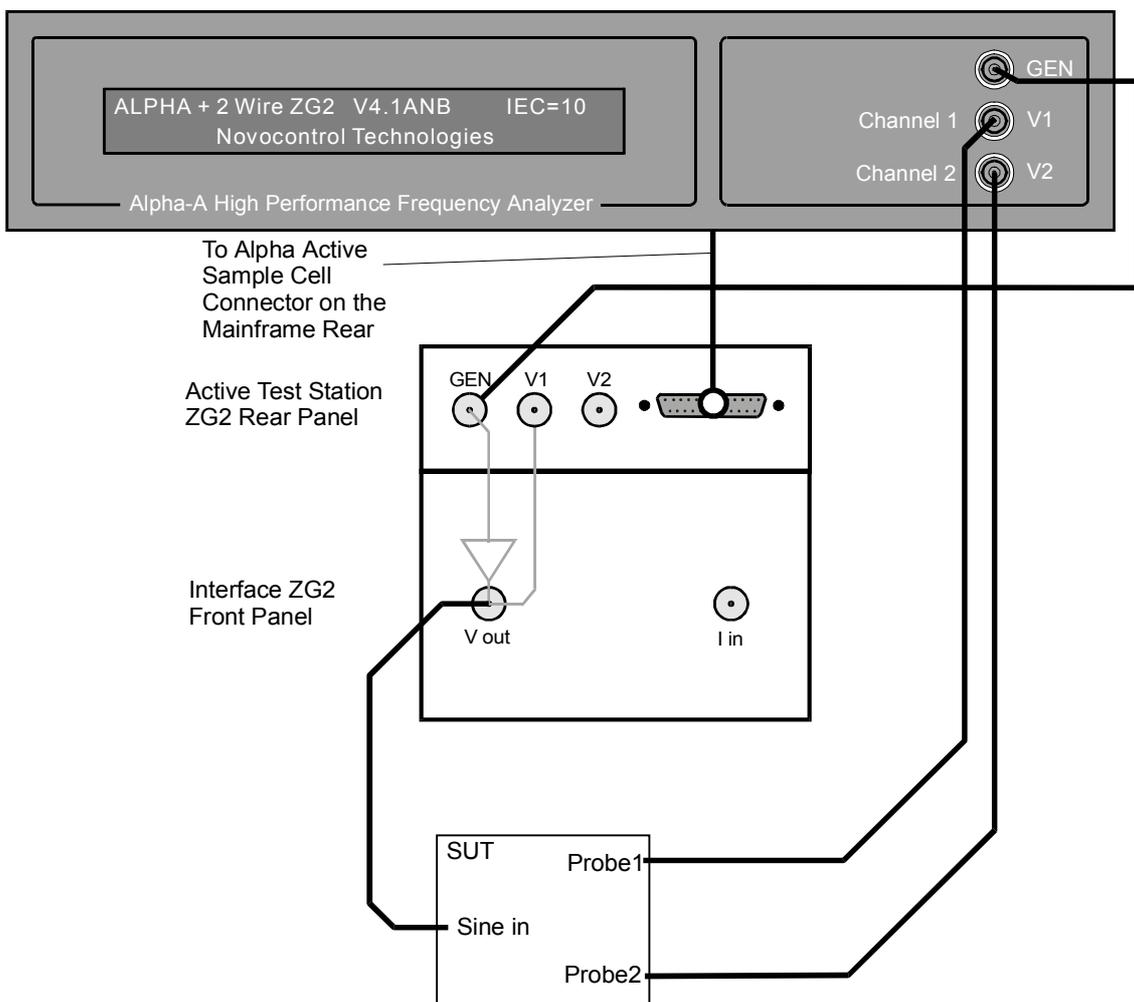


Fig. 25. Interface ZG2 connections to the Alpha main frame in gain phase mode.

Important: For the GEN, V1 and V2 connections use only the 1m BNC cables supplied by Novocontrol. Usage of cables with other wave impedance or length may reduce accuracy.

8.4. Potentiostat Galvanostat Electrochemical Interfaces POT/GAL 30V 2A and POT/GAL 15V 10A

These interfaces are described in the Novocontrol "POT/GAL 30V 2A" and "POT/GAL 15V 10A Electrochemical Impedance Potentiostat Galvanostat Test Interface for Alpha-A Analyzer" manuals which are supplied with the interface. An overview is given in the "Introduction" chapter.

9. Test Interfaces for Dielectric, Conductivity and Impedance Measurements

Test interfaces extend the performance of the Alpha analyzer mainframe. An overview on the available test interfaces is given in the "Introduction" chapter.

9.1. High Voltage Interfaces HVB300, HVB 1000 and HVB4000

These interfaces are described in the Novocontrol "High Voltage 300 Vpp Test Interface HVB300", "High Voltage 1000 Vpp Test Interface HVB1000" and "High Voltage 4000 Vpp Test Interface HVB4000" manuals which are supplied with the interfaces. An overview is given in the "Introduction" chapter.

10. Test Interfaces for Gain Phase Measurements

Test interfaces extend the performance of the Alpha analyzer mainframe. An overview on the available test interfaces is given in the "Introduction" chapter.

10.1. 2 Differential Channel High Input Gain Phase Interface G22

This interface is described in the Novocontrol "2 Differential Channels High Input Gain Phase Interface G22" manual which is supplied with the interface. An overview is given in the "Introduction" chapter.

11. Setting up the Alpha Analyzer for Measurement

11.1. System Requirements

The Alpha analyzer has to be operated by control software on a separate host computer via the GPIB IEEE 488 bus.

You can either use standard software from Novocontrol or own written software.

If you intend to control the Alpha by own software, refer to the "GPIB IEEE 488 Interface" chapter. The following components are required.

- A standard software development tool like e.g. a Basic interpreter or C compiler.
- A host computer with an GPIB IEEE 488 interface port. The computer and the IEEE 488 interface must match to the software development tool.
- If you do not have an active sample cell ZGS for electric material measurements a suitable sample cell is required. The Novocontrol BDS 1200 sample cell is recommended.

The Novocontrol WinDETA / WinIMP software supports dielectric, conductivity and impedance measurements with optional support of temperature control. You must have the following components in order to operate the Alpha by WinDETA or WinIMP.

- The WinDETA or WinIMP software package from Novocontrol GmbH.
- Either a Novocontrol GPIB PCI card or a National Instruments GPIB board matching the MS-Windows system for remote control of the Alpha analyzer.
- An IBM compatible PC with a 486 or higher processor with at least 16 MB memory and MS-Windows 95, 98 or NT operating system. A PC with a Pentium processor is recommended.
- If you do not have an active sample cell ZGS, for electric material measurements a suitable sample cell is required. The Novocontrol BDS 1200 sample cell is recommended.
- If sample temperature control is required: The Novocontrol WinDETA software, a Novocontrol temperature control system based on the QUATRO, Novocool, or Novotherm controller or another temperature control system based on an Eurotherm 818 or 2400 series temperature controllers.

11.2. Performing a Dielectric, Conductivity or Impedance Measurement

- If you have a Novocontrol software package for electric material and impedance measurements, install it on your PC. For details, follow the instructions of the installation program and the manual.
- If you intend to program the Alpha analyzer by yourself, refer to the "GPIB IEEE 488 Interface" chapter.
- Connect one of the test interfaces to the Alpha mainframe and set up all required connections as described the previous chapters.
- Connect a sample or sample cell to the test interface as described in the "Connections for Dielectric, Conductivity or Impedance Measurement" chapters of the several interfaces.

- If you have an active sample cell ZGS cell or a Novocontrol BDS 1200 sample cell, mount the sample between the electrodes. For details refer to the "Sample Preparation" chapter and follow the instructions of the WinDETA manual.
- If you intend to use an own dielectric sample cell for a test interface different from the active cell ZGS, refer to the "Using an Own Dielectric Sample Cell for Impedance Measurements" chapter for details.
- Start the software and follow the manual instructions for setting up and starting a measurement.

Note: After switching the Alpha mainframe on, it will show its first boot message after about 10 seconds initial internal boot time. Refer to the "Alpha mainframe Front Panel" chapter for details.

11.3. Performing a Gain Phase Measurement

- If you have a Novocontrol software for gain phase measurements, install it on your PC. For details, follow the instructions of the installation program and the manual.
- If you intend to program the Alpha analyzer by yourself, refer to the "GPIB IEEE 488 Interface" chapter.
- If you want to use a test interface for gain phase measurements, connect it to the Alpha mainframe as described in the previous chapters.
- Connect the sample or system under test to the Alpha as described in the "System Setup for Gain Phase Measurement " chapters.
- Start either the Novocontrol software for frequency response measurements or your own software and follow the instruction of the manual for setting up and starting a measurement.

Note: After switching the Alpha mainframe on, it will show its first boot message after about 10 seconds initial internal boot time. Refer to the "Alpha mainframe Front Panel" chapter for details.

12. Display

The Alpha analyzer display gives information on the actual state of measurement and shows the data of the last measured point. After switching the instrument on, or after a GPIB **RSTH** command, the display shows the two start up message as described in the "Instrument Description, Alpha Mainframe, Front Panel" chapter. Depending on the mode of operation, the following information is provided after a measurement is started.

12.1. Display for Dielectric, Conductivity or Impedance Measurements

After starting a measurement at a single frequency, the display shows the various states of the measurement procedure as follows :

15. Principles of Operation

15.1. Frequency Response Analyzer

The Alpha mainframe incorporates a digital Frequency Response Analyzer (FRA) with sine wave generator, dc bias generator and two analysis channels. The FRA is used in combination with a current to voltage converter as described in the next chapter for dielectric or impedance measurements. The FRA may be used for stand alone frequency response analysis (gain phase measurements), too.

The FRA measures the response of a system to a harmonic (sinusoidal) excitation. The excitation signal and the response signal are voltages. Other physical quantities may be measured too, if they are derived from a voltage (excitation signal) or converted into a voltage (response signal).

The response signal is analyzed by Fourier transform. One is especially interested in the amplitude of the sinusoidal base wave (0. harmonic) and the phase angle of the base wave with respect to the excitation signal. The measurement is generally not done only at one fixed frequency point, but instead a sequence of frequencies are measured in order to create a frequency sweep over a wide range.

For many applications, it is required to measure two voltages at two arbitrary points of a system under test (SUT) with respect to each other at the frequency of the generator signal. Therefore, the Alpha analyzer contains two independent voltage input channels and correlators as shown below.

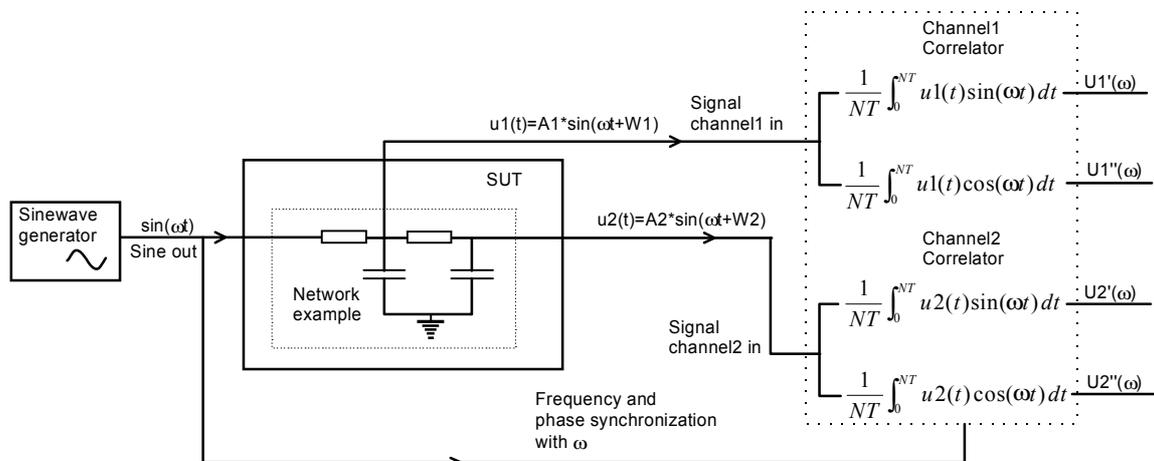


Fig. 30. Basics of frequency response analysis.

A sine wave generator creating the excitation signal is connected to the system under test (SUT). The SUT may be of any electrical system type with an input for the FRA generator signal and one or two electrical points of interest which can be connected to the FRA inputs. In fig. 30, a RC network is shown as an example. The input signals $u_1(t)$ and $u_2(t)$ are applied to a correlator performing the Fourier transform. The correlators are phase synchronized to the generator, so that the correlation frequency $\omega/2\pi$ corresponds to the generator frequency and a defined phase relation between the generator and the correlators exists.

The response of correlator 1 to the signal $u_1(t)$ are the two constant (not time dependent) signals

$$U_1'(\omega) = \frac{2}{NT} \int_0^{NT} u_1(t) \sin(\omega t) dt \quad (5)$$

$$U_1''(\omega) = \frac{2}{NT} \int_0^{NT} u_1(t) \cos(\omega t) dt \quad (6)$$

where U_1' is the in phase component and U_1'' the orthogonal (90° shifted, quadratur) component of the harmonic base wave of $u_1(t)$. N is the number of periods with duration $T=2\pi/\omega$ measured by the correlator.

The amplitude $A_1(\omega)$ and phase angle $W_1(\omega)$ (with respect to the generator) of the base wave of $u_1(t)$ is calculated from

$$A_1(\omega) = \sqrt{U_1'^2 + U_1''^2} \quad (7)$$

$$W_1(\omega) = \arctan\left(\frac{U_1''}{U_1'}\right) \quad (8)$$

Corresponding equations apply for correlator 2 and the signal $u_2(t)$. In gain phase mode, the GPIB **MRE?** command returns the three parameters %f1 = $U_1'(\omega)$, %f2 = $U_2'(\omega)$ and %f3 = $U_2''(\omega)$. Channel 1 is internally used as the phase reference channel and therefore the phase angles of both channels are normalised to $W_1=0^\circ$ corresponding to $U_1''(\omega) = 0$.

For readers having no experience in Fourier analysis, the following may be helpful in order to get a feeling for the operation of the correlator. If $u_1(t)$ is a sine wave with

$$u_1(t) = A_1 \sin(\omega t + W_1),$$

the product

$$u_1(t) \sin(\omega t) = A_1 \sin(\omega t + W_1) \sin(\omega t) = \frac{A_1}{2} ((\cos(W_1) - \cos(2\omega + W_1))). \quad (9)$$

(For the second = , $\sin(x) \sin(y) = (\cos(x-y) - \cos(x+y))/2$ was used.) (10)

As the integration in (5) is performed over a number of complete periods, the second term in eq. (9) averages out to zero. Therefore, the integral (5) becomes $U_1'(\omega) = A_1 \cos(W_1)/2$. With the same arguments, $U_1''(\omega) = A_1 \sin(W_1)/2$. From this, eq. (7) and (8) follow immediately.

If $u_1(t)$ is a signal of arbitrary type, it can be transformed into its Fourier representation consisting of a number of sine waves with any kind of frequencies. In this case, for each frequency component both terms of eq. (9) are frequency dependent and will average out to zero, if the integration is performed over a large number of periods. The only frequency component which does not average out, is the one at the frequency ω of the correlator.

Therefore the correlator phase sensitive detects the base Fourier component contained in any input signal. All other contributions are suppressed (averaged out). The quality of the suppression increases with averaging time (number of periods N of the integration). Therefore,

this technique generally is used in precision instrumentation for noise suppression or if very small signals have to be measured (lock in amplifiers). E.g. measuring a signal in the nV range superimposed by a 1000 times larger noise signal is possible.

A principal drawing of the Alpha frequency response analyzer unit is shown in fig. 31. The ac generator signal is directly digitally synthesized by a sine wave synthesizer. The sine wave synthesizer continuously calculates digitally values of the sine wave function at the actual frequency and amplitude. This digital data stream is converted by a high speed digital to analog converter to an analog stepped sine wave.

The signal is then applied to a low pass filter in order to remove the sine wave step components. The sine wave passes a level shifter in order to superimpose an additional dc (bias) voltage. The level shifter maybe bypassed by the Bias On / Off selector. The signal is next fed to the output amplifier and connected to the GEN signal output plug by a 50 Ω resistor.

After passing the sample under test (SUT) the two signals Probe 1 and Probe 2 are applied to the input channels by the plugs V1 and V2.

The input impedance of each input channel is 1 M Ω in parallel with < 10 pF capacity. The input channels maybe dc or ac coupled by the "AC / DC Coupling" selector.

Note : If ac coupling is enabled, the de coupling capacitor acts as an additional high pass filter which results to a significant decrease of the measured amplitude and a phase deviation at frequencies below approximately 1 Hz. These effects are not compensated by the Alpha analyzer and should be considered by the user.

Next, the input signal is applied to an input amplifier with the following ranges.

Input Range	Max. Input Voltage [Vrms]
8	3.2
7	1.7
6	1
5	0,56
4	0,32
3	0,17
2	0,1
1	0,056
0	0,032

Tab. 4. Voltage ranges of each input channel of the Alpha mainframe

The amplified signal passes the low pass filter. It suppresses frequency components above the half sampling frequency of the following analog to digital converter. The analog signals are converted into a continuous digitally data stream representing the wave form applied to the input channels. The digital data are continuously read by the micro processor which applies a discrete Fourier transform to the data. The incoming data points are multiplied according to eqn. (5) and (6) by digital reference sine and cosine waves and then summed up for the calculation of $U1'(\omega)$, $U1''(\omega)$, $U2'(\omega)$, $U2''(\omega)$, for the two channels. Finally the amplitudes of the harmonic bas waves $A1(\omega)$ and $A2(\omega)$ and their phase difference $W1(\omega) - W2(\omega)$ are calculated by eqn. (7) and (8).

All functions of the Alpha analyzer frequency response analyzer unit are operated by the IEEE 488 port of an external computer. Refer to chapter "GPIB IEEE 488 Interface" for details.

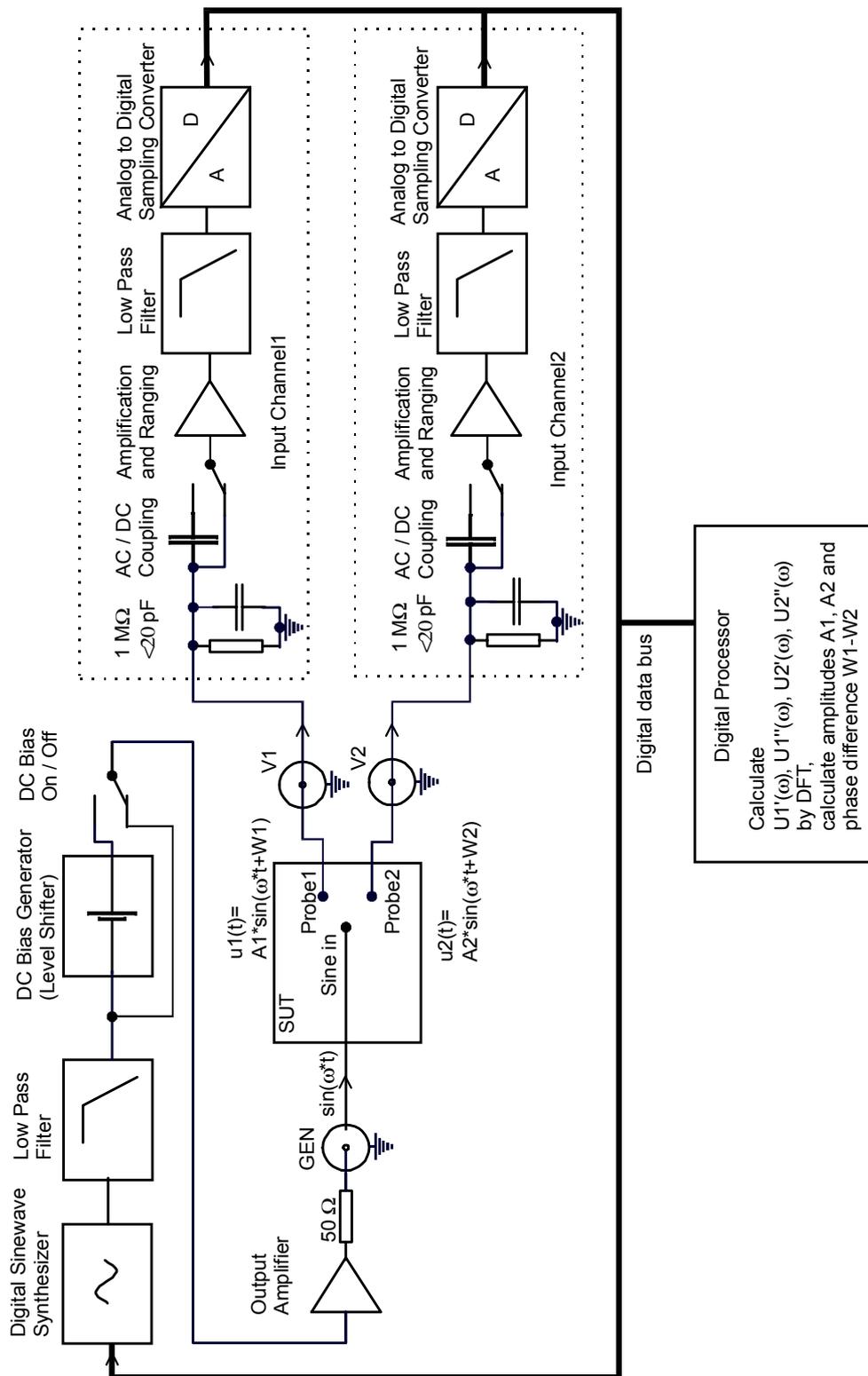


Fig. 31. Main building blocks of the Alpha frequency response analyzer part.

15.2. Current to Voltage Converter

For dielectric, conductivity or impedance measurements, the voltage applied to the sample and the response current to the applied voltage have to be measured. For details refer to the "Principle of Dielectric, Conductivity and Impedance Measurement" chapter.

The sample voltage can be measured directly with the first channel of the Alpha frequency response analyzer (FRA). In order to measure the sample current, an additional current to voltage converter is used which converts the sample current into a voltage measured by the second Alpha FRA channel. The current to voltage converter is usually mounted in a test interface in order to have it located close to the sample.

The measurement principle of the current to voltage converter is shown below:

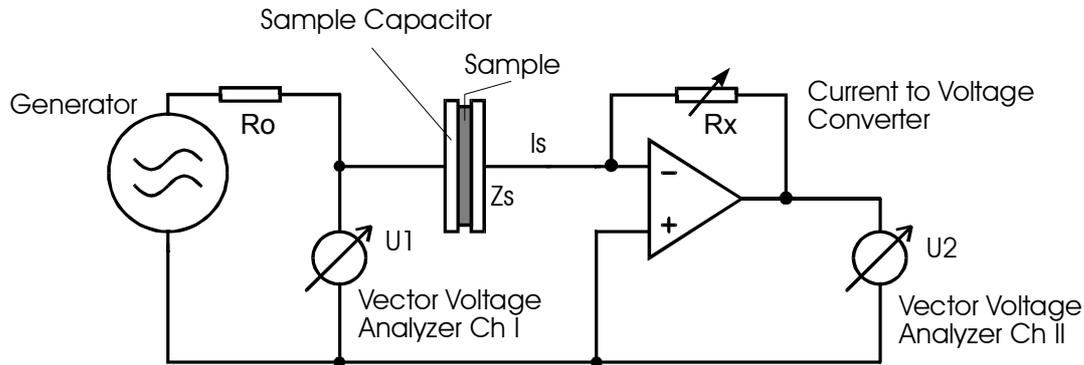


Fig. 32. Principle of the impedance measurement.

The ac voltage from the generator is applied to the sample and measured in amplitude and phase as U_1 . The resistor R_o limits the sample current if the sample impedance becomes too low. The sample current I_s feeds in the inverting input of an operational amplifier which has the variable resistor R_x in its feedback loop. The Alpha analyzer selects a R_x value so that the output voltage U_2 of the operational amplifier is in a good measurable range of the voltage input channels. For ideal components, U_2 is related to the sample current I_s with

$$I_s = -\frac{U_2}{R_x} \quad (11)$$

For an ideal operational amplifier (infinite open loop gain), the voltage at the I_s input is 0V with respect to ground (virtual ground with zero input impedance at the current input) and therefore U_1 corresponds to the voltage over the sample capacitor. Under these precautions, the sample impedance Z_s is calculated from

$$Z_s = \frac{U_1}{I_s} = -\frac{U_1}{U_2} R_x \quad (12).$$

Depending on the test interface the built-in operational amplifier can sense extreme low input currents down to fA and therefore the performance for measuring high impedance is good. This performance is combined with wide bandwidth up to 10 MHz.

15.3. Reference Measurement

The principle of reference measurement is shown below. After each sample measurement the current to voltage converter is switched to the variable reference capacitor and a second reference measurement is done.

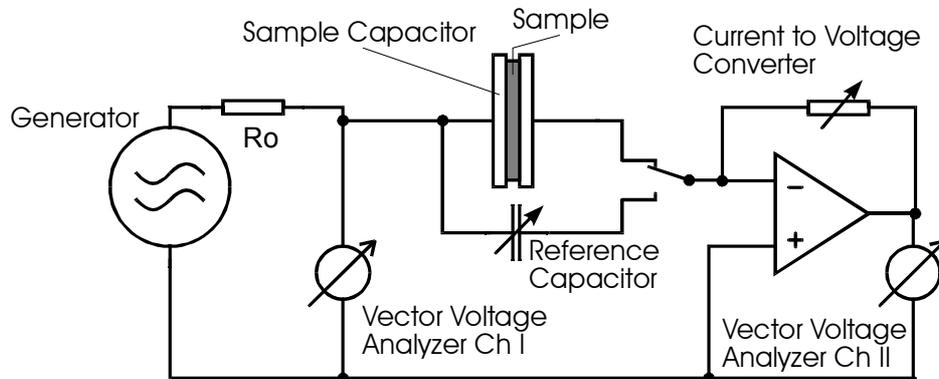


Fig. 33. Principle of reference measurement.

The reference measurement is used in order to do a kind of online calibration of the current to voltage converter with respect to the reference capacitor. This technique improves accuracy significantly as all linear systematical deviations of the current to voltage converter and the following FRA channels are cancelled out.

Nevertheless, some sources of errors as e.g. non linear distortions remain active. These effects can be minimised, if the difference between sample and reference impedance is kept small. In this case, the analyzer measures nearly identical values for the sample and the reference measurement and the measurement is only limited by the analyzer resolution (the accuracy for reproducing values at constant input voltage).

In practise, non linear errors occur if the sample impedance differs more than 20 % from the reference impedance. Therefore, for most test interfaces the reference impedance can be adjusted to several values. In the auto reference mode, the Alpha will select automatically the reference capacity which matches the sample best.

The following modes for reference measurement are supported.

- Measurement **without reference**. In this mode, the basic accuracy of the sample impedance is limited to about 0.2% and decreases especially at high frequencies.
- Measurement with reference and **auto reference mode**. In this mode, for each impedance point first the sample is measured. From this value, the reference capacity with the lowest difference of impedance to the sample is selected and Z_S is recalculated with enhanced precision as specified in the "Measurement ranges and Accuracy, Accuracy of Impedance Measurement" chapter. This mode results in highest overall accuracy.
- Measurement with **fixed reference**. In this mode, the reference capacity is selected by the user and not automatically changed. This may be useful, if highest resolution in capacity is required. In this case its more convenient to use a fixed reference capacity, as the automatic

switching of the reference capacities may induce small steps in the result, which can be up to 10^{-4} of the measured capacity.

The different reference modes can be selected by the Alpha GPIB **ZREFMODE=** command or by Novocontrol WinDETA software dialogue Analyzers, Options Alpha, Configuration.

15.4. Higher Harmonics Measurement

As described in the "Principles of Operation, Frequency Response Analyzer" chapter, the input signals $u1(t)$ and $u2(t)$ at the Alpha input channels V1 and V2 are applied to two correlators. Each correlator detects the two orthogonal components of the harmonic base wave contained in the corresponding input signal. E.g. for the first channel and $u1(t)$

$$U1'_n(\omega) = \frac{2}{NT} \int_0^{NT} u1(t) \sin(n\omega t) dt \quad (18)$$

$$U1''_n(\omega) = \frac{2}{NT} \int_0^{NT} u1(t) \cos(n\omega t) dt \quad (19)$$

where for $n = 1$, $U1'_1$ is the in phase component and $U1''_1$ the orthogonal (90° shifted, quadratur) component of the harmonic base wave of $u1(t)$. N is the number of periods with duration $T = 2\pi/\omega$ measured by the correlator.

Usually $u1(t)$ is the response signal of a system under test (SUT) to the Alpha sine wave generator at frequency $\omega/2\pi$. Refer to the "Principles of Operation, Frequency Response Analyzer" chapter for details.

If the SUT is linear, the response $u1(t)$ will be like the Alpha generator signal a pure sine wave, too. Both the generator - and response signal $u1(t)$ may contain some additional noise which may add other frequency components to $u1(t)$. One correlator purpose for linear SUTs is to suppress this noise and reduce the response signal to its harmonic base contributions.

On the other hand, if the SUT is non linear, the response signal will be not a pure sine wave but will contain additional components at multiple frequencies of the generator excitation frequency $\omega/2\pi$. The additional frequency components are called higher harmonics. The frequency component at n times the base frequency $\omega/2\pi$ is called the $n-1$ harmonic. Each harmonic is characterized by an amplitude and phase angle with respect to the base wave as shown below.

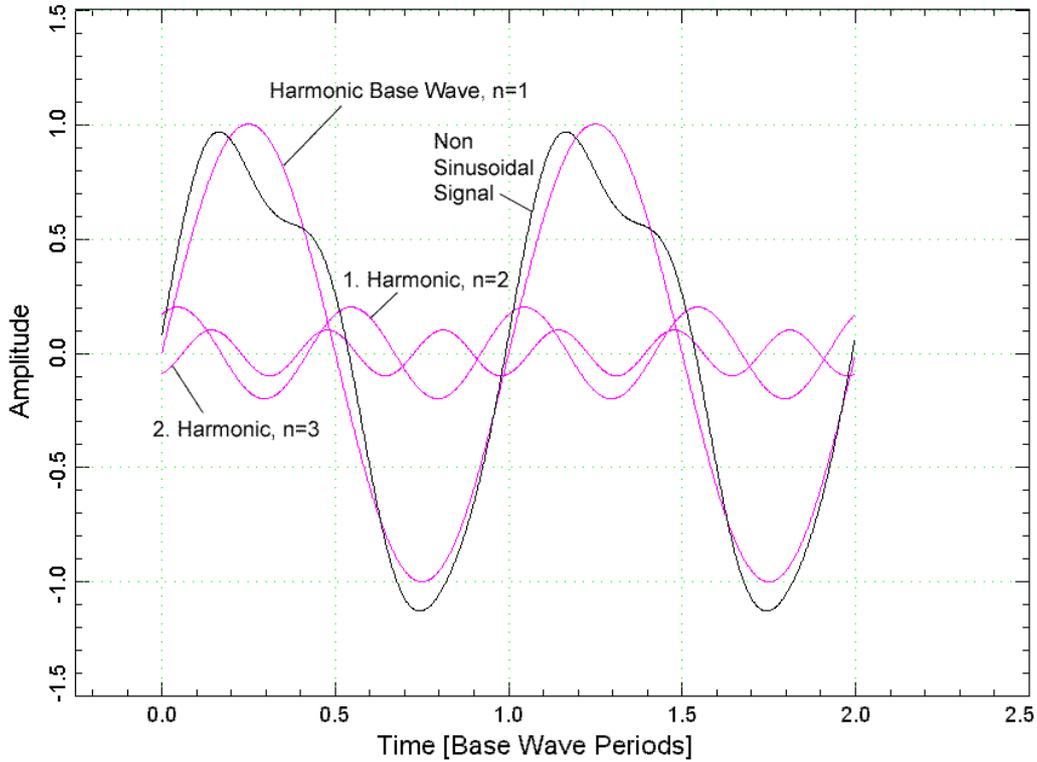


Fig. 34. Non sinusoidal signal and its harmonic components.

The total non sinusoidal input signal is summed up by all harmonics components

$$u_1(t) = \sum_{n=1}^m U_1' \sin(n\omega t) + U_1'' \cos(n\omega t) \quad (20)$$

where $m-1$ denotes the highest harmonic contained in the input signal.

For harmonics with frequencies $n \omega / 2\pi \leq 1500$ Hz, the Alpha can measure both sin and cos parts U_1' and U_1'' . For harmonics with frequencies > 1500 Hz, only the harmonics absolute values

$$|U_1| = \sqrt{U_1'^2 + U_1''^2} \quad (21)$$

of all harmonics up to the highest generator frequency are measured. For channel 2 and $u_2(t)$ corresponding equations apply.

Measurement of harmonics is supported by WinDETA software in impedance mode. For details refer to the WinDETA manual.

The Alpha internal command set supports harmonics measurement both for gain phase and impedance mode. For both modes, harmonics measurement must be enabled by the **SHM=** command before starting a measurement. After this, the following commands may be used after

each measurement point started by the **MST** command in order to detect the harmonics as a relative portion of the harmonic base wave absolute value.

Use **CHM=** in order to select the output format of the following harmonics query commands described below. **CHM=0** selects output of only harmonic absolute values. **CHM=1** selects output of harmonics both sin and cos parts for harmonic frequencies ≤ 1500 Hz.

In the following %fk denotes the k-th return parameter of a GPIB query command (k=1, 2, 3, ...).

In gain phase mode:

The **MRE?** command returns the base wave parameters

$$U1'_1 = \%f1, U1''_1 = 0 \text{ by normalisation, } U2'_1 = \%f2, U2''_1 = \%f3.$$

If **CHM? = 0** the **HMS1?** command returns the harmonics absolute values normalised to the $u1(t)$ base wave

$$|U1_n|/|U1_1| = \%fn-1, \quad n = 2, 3, \dots, m.$$

$$\text{E.g. } |U1_2|/|U1_1| = \%f1, \quad |U1_3|/|U1_1| = \%f2, \dots$$

If **CHM? = 1** the **HMS1?** command returns the harmonics sin and cos parts normalised to the $u1(t)$ base wave absolute value

$$U1'_n/|U1_1| = \%f(2(n-1)-1); \quad U1''_n/|U1_1| = \%f(2(n-1)), \quad n = 2, 3, \dots, m.$$

$$\text{E.g. } |U1'_2|/|U1_1| = \%f1; \quad |U1''_2|/|U1_1| = \%f2, \quad |U1'_3|/|U1_1| = \%f3; \quad |U1''_3|/|U1_1| = \%f4, \quad \dots; \dots$$

For harmonic frequencies $F_n = n * \omega/2\pi > 1500$ Hz,

$$|U1_n|/|U1_1| = \%f(2(n-1)-1); \quad 0 = \%f(2(n-1)).$$

$$\text{E.g. } |U1_4|/|U1_1| = \%f5; \quad 0 = \%f6, \quad |U1_5|/|U1_1| = \%f7; \quad 0 = \%f8, \quad \dots; \dots$$

The **HMS2?** command returns corresponding values for $u2(t)$ at channel 2. All normalizations are done to the absolute value of the $u2(t)$ base wave $|U2_1|$.

In impedance mode:

The sample voltage $us(t)$ corresponds to the channel 1 voltage $u1(t)$. Corresponding to (20) the sample voltage and current

$$us(t) = \sum_{n=1}^m Us'_n \sin(n\omega t) + Us''_n \cos(n\omega t)$$

$$is(t) = \sum_{n=1}^m Is'_n \sin(n\omega t) + Is''_n \cos(n\omega t) .$$

The **ZEXTRE?** command returns the base wave parameters of the sample voltage measurement

$$Us'_1 = \%f9, \quad Us''_1 = 0 \text{ by normalisation.}$$

The sample current base wave is determined from the sample impedance Zs by

$$Is'_1 = \text{Re}(U1/Zs), \quad Is''_1 = \text{Im}(U1/Zs), \quad \text{with } Zs = \%f3 + j \%f4 \text{ or } Zs = \%f5 + j \%f6.$$

If **CHM? = 0** the **ZHMSVS?** command returns the sample voltage harmonics absolute values normalised to the base wave

$$|Us_n|/|Us_1| = \%fn-1, \quad n = 2, 3, \dots, m.$$

If **CHM? = 1** the **ZHMSVS?** command returns the sample voltage harmonics sin and cos parts normalised to base wave absolute value

$$Us'_n/|Us_1| = \%f(2(n-1)-1), \quad Us''_n/|Us_1| = \%f(2(n-1)), \quad n = 2, 3, \dots, m.$$

For harmonic frequencies $F_n = n * \omega/2\pi > 1500$ Hz,

$$|Us_n|/|Us_1| = \%f(2(n-1))-1, \quad 0 = \%f(2(n-1)).$$

If **CHM? = 0** the **ZHMSIS?** command returns the sample current harmonics absolute values normalised to the base wave

$$|Is_n|/|Is_1| = \%fn-1, \quad n = 2, 3, \dots, m.$$

If **CHM? = 1** the **ZHMSIS?** command returns the sample current harmonics sin and cos parts normalised to base wave absolute value

$$|s'_n|/|s_1| = \%f(2(n-1)-1), \quad |s''_n|/|s_1| = \%f(2(n-1)), \quad n = 2, 3, \dots, m.$$

For harmonic frequencies $F_n = n * \omega/2\pi > 1500$ Hz,

$$|s_n|/|s_1| = \%f(2(n-1)-1), \quad 0 = \%f(2(n-1)).$$

If reference measurement is activated, the **ZEXTRE?** command returns the base wave parameters of the reference capacitor voltage measurement

$$Ur'_1 = \%f12, \quad Ur''_1 = 0 \text{ by normalisation.}$$

The reference capacitor current base wave is determined from the capacitor impedance Z_r by

$$Ir'_1 = \text{Re}(Z_r), \quad Ir''_1 = \text{Im}(Z_r), \quad \text{with } Z_r = -j / (\omega Cr), \quad Cr = \%8, \text{ and } \omega = 2\pi \text{ base frequency.}$$

The **ZHMSVR?** and **ZHMSIR?** commands return the corresponding values of **ZHMSVS?** and **ZHMSIS?** for the reference capacitor harmonics voltage and current components. Harmonic voltages are normalised to $|Ur_1|$, harmonic currents are normalised to $|Ir_1|$.

The accuracy of harmonics measurements is limited by two factors.

1. The correlator accuracy according (18) and (19). The absolute correlator error for a higher harmonic U_{1n} is the same as the error of a harmonic base wave $U_{11}(n * \omega/2\pi)$ at the frequency $n * \omega/2\pi$ as specified in the "Measurement Ranges and Accuracy" chapter. As the harmonics are usually smaller than the base wave, the relative error of the higher harmonics increases with the ratio $U_{11}(\omega)/U_{1n}$.

2. The generator signal contains higher harmonic components due to analog and digital noise of about 0.1% of the base wave for generator voltages between 3V .. 0.3V. For lower voltages, the error linearly increases. These higher harmonics are applied to the SUT and will be contained in the response voltages or currents, too.

15.5. 3- and 4-Wire Impedance Measurement

The principle of a four wire impedance measurement is shown below. The difference between the 2-wire measurement were both sample voltage U_s and current I_s are measured with two wires is that in a 4-wire measurement two additional wires **V high** and **V low** are used in order to measure the sample voltage. The remaining two wires apply the electrical sine wave to the sample (**I high**) and measure the sample current (**I low**).

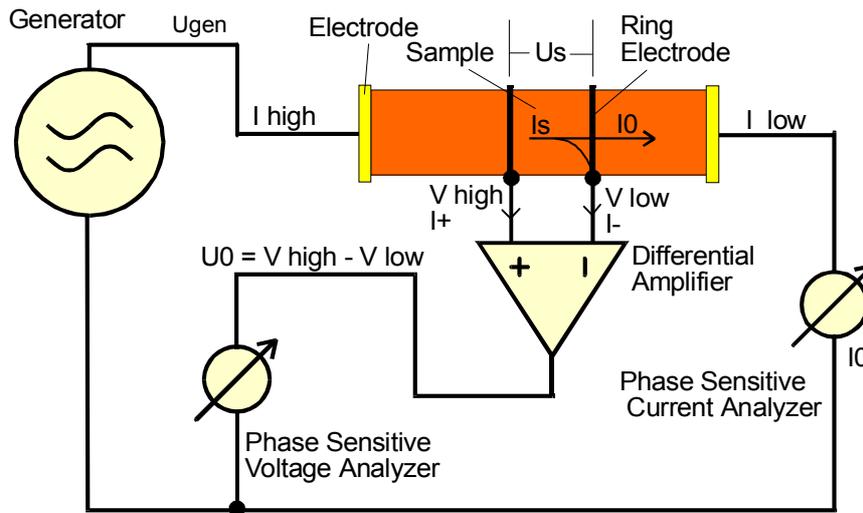


Fig. 35. Principle of 4-wire impedance measurement

The sample impedance between the two ring electrodes is defined by

$$Z_s^* = \frac{U_s}{I_s}$$

where *U_s* is the voltage and *I_s* the current in the volume between the ring electrodes. For an ideal system, the voltage inputs have infinite impedance and no currents *I₊*, *I₋* flow into the voltage terminals **V high**, **V low** (*I₊* = *I₋* = 0). In this case (and only in this case) the sample current *I_s* corresponds to the measured current *I₀* and the measured voltages **V high**, **V low** correspond to the internal sample voltages at the position of the electrode rings. In this case, the sample impedance can be calculated by

$$Z_s^* = \frac{U_0}{I_0} = \frac{V_{high} - V_{low}}{I_0}$$

For a linear sample, *Z_s** is independent from the impedance of the sample parts left and right from the two ring electrodes, the contact impedance and the impedance of the **I high** and **I low** wires.

Therefore, four wire measurements may be useful in the following cases.

- If it is difficult to apply proper contacts with defined and low resistance to the sample or a zone of an inhomogeneous sample. An example would be e. g. an ion conductor with metal contacts. In this case electrode or interface polarization effects may contribute a major unwanted effect to the measured impedance. With a four wire setup, the electrode effects can be partly suppressed.
- If the impedance of the contacts and the wires connected to **I high** and **I low** are not small against the sample impedance.

In practice, systems are not ideal and currents will flow into the **V high** and **V low** terminals. This results in two kind of errors.

- The measured sample current I_0 deviates from the true sample current I_s by the current I_- flowing in the **V high** terminal. The current I_+ flowing in the **V high** terminal does not affect the sample current measurement accuracy.
- The voltages measured at **V high** will deviate from the true voltage at the position of the electrode by the contact voltage $U_c = I_+ \cdot \text{contact impedance}$. The same effect applies to the voltage measured at **V low**.

Therefore, for 4-wire measurements one should always make sure that

- the current I_- of the **V low** terminal is small against the measured current and
- the contact voltages at the **V high** and **V low** voltages (due to the currents I_+ , I_- multiplied by the contact impedance) are small against the measured differential voltage **V high - V low**.

For the 4-wire test interface ZG4, the input current of each voltage terminal has three components.

- The dc bias of current I_b current caused by the differential amplifier electronics which is < 2 pA.
- The current caused by the differential amplifier input impedance which can be approximately modelled by a capacity $C_{amp} < 10$ pF in parallel with a resistance $R_{amp} > 1$ Tohm.
- The parallel impedance of the BNC cable which connects the ring electrode with the active interface **V high** terminal. This impedance is caused by the capacity C_{cab} and isolation resistance R_{cab} of the volume between the inner cable conductor and the outer shield. The capacity is about 120 pF / m cable length, the resistance depends on the cable quality and is proportional to 1 / cable length, too. For good cables with length < 1 m, the cable resistance (but not the capacity) can usually be neglected against the amplifier resistance R_{amp} .

With this, the total input current on the **V high** terminal is approximately

$$I_{+dc} = V_{+dc} / R_{amp} + I_b$$

$$I_{+ac} = V_{+ac} \left(\frac{1}{R_{amp}} + j\omega(C_{amp} + C_{cab}) \right)$$

where I_{+dc} and V_{+dc} are the dc current and voltage components at the terminal, I_{+ac} and V_{+ac} the ac components, j imaginary unit, $\omega = 2\pi$ frequency. For the **V low** terminal corresponding equations apply. The cable capacity can be partly compensated by the driven shield setup described in the next chapter.

The ZG4 and POT/GAL test interfaces can be configured for 2, 3 and 4 wire setups as described in the "4 Wire Impedance Interface ZG4" chapter.

15.6. Driven Shields Setup for 3- and 4-Wire Impedance Measurements

As discussed in the "4-Wire Impedance Measurement" chapter, in 3- or 4-wire mode the parallel cable impedance of the voltage inputs **V high** and **V low** result in an unwanted load current I_{shield} to which may contribute to the measured sample impedance. This current is caused by the potential difference between the parallel capacity and resistance of the inner cable conductor with respect to the outer cable shield conductor.

The current I_{shield} can be minimised, if the potential difference of the inner conductor to the shield is kept small. This can be realized by keeping the shield potential at the same potential as the inner conductor.

The setup for the interfaces ZG4 and POT/GAL which support driven- and not driven shield mode is shown below. In driven shield mode, a high input and low output impedance voltage follower (unity gain amplifier) isolates the shield from the inner conductor while keeping it at the inner conductor potential.

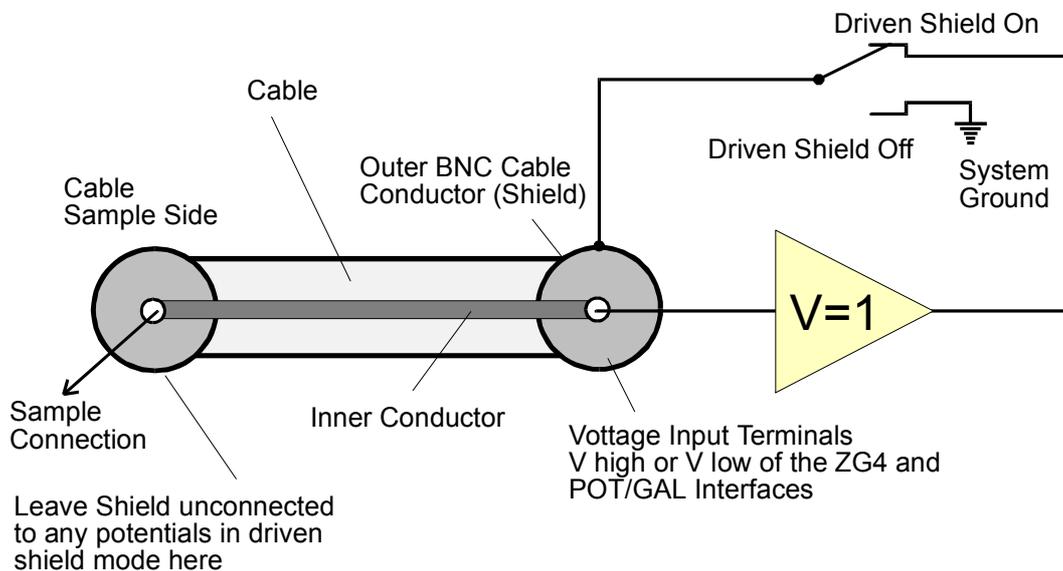


Fig. 36. Interfaces ZG4 and POT/GAL voltage input configuration for the V high or V low terminals with and without driven shield mode.

In practice, the setup in fig. 36 in driven shield mode reduces cable capacity by about one order of magnitude at low frequencies below 300 kHz.

On the other hand at high frequencies in the MHz range, problems arise as the signal applied at the inner conductor sample side has to travel through the cable, the driven shield and back through the shield to the sample side shield end. This consumes a certain time which at high frequencies cause a phase shift between the inner conductor and the shield. The phase shift results in an increased shield current which can even extend the shield current without driven shield setup or result in not controlled oscillations. In order to prevent this, the shield driver current is continuously reduced for frequencies exceeding about 1 MHz.

Therefore in driven shield mode at low frequencies the inner cable conductor input impedance at the sample side is nearly reduced to the interface input impedance which is about $10 \text{ pF} \parallel 1 \text{ T}\Omega$ for the ZG4 and POT/GAL interfaces. At high frequencies, the cable capacity of about $120 \text{ pF} / \text{m}$ BNC cable has to be added to the 10 pF input capacity. The driven shield setup reduces input impedance at low frequencies, but may result in additional frequency response at high frequencies in the measured sample impedance.

The driven shield mode can be activated independent for the **V high** and **V low** terminal by the Alpha **DRS=** GPIB command or from the WinDETA by "Analyzers, Configuration (Alpha Analyzer), Driven Shields".

22. Technical Data

Alpha Mainframe

Line voltage :	220 - 240 V ac, 50 - 60 Hz or 110 V ac, 50 - 60 Hz (see instrument rear)
Power consumption :	< 100 W
Environment	
operating temperature :	0° to 40°C
storage temperature :	-10° to 60°C
specification limits :	15° to 25°C
GPIB IEEE 488 interface	
can be addressed as :	talker / listener
pre set device address :	10

Mainframe frequency response analyzer unit

Two voltage input channel digital frequency response analyzer with sine wave and dc-bias generator

Voltage input channels 1 and 2

Frequency range

3 μ Hz .. 40 MHz ac or dc coupled

Voltage ranges (V_{rms}) :

3.2 V, 1.7 V, 1 V, 560 mV, 320 mV, 170 mV,
100 mV, 56 mV, 32 mV

Amplitude and phase resolution and accuracy

See chapter "Measurement Ranges and Accuracy, Accuracy of Gain Phase Measurement"

Input impedance

Resistance : 1 M Ω , Capacity < 100 pF

Measured parameters

Dc, ac base and higher harmonic components V1*, V2* of the both input channels at generator frequency, phase angle of (V1*, V2*)

Measurement rate:

Up to up to 157 impedance or 210 gain phase data points per second via GPIB port with mainframe option F (high speed).

Up to 10.5 impedance or 19 gain phase data points per second via GPIB port without option F.

Mainframe sine wave generator

Principle of operation

Direct digitally synthesized from 3 μ Hz .. 0.3, 3, 20, or 40 MHz for Alpha-AL, -AK, -AN or -AT

Frequency resolution

23 mHz for 40 MHz .. 20 MHz

12 mHz for 20 MHz .. 1.25 MHz
 0.73 mHz for 1.25 MHz .. 78 kHz
 45 μ Hz for 78 kHz .. 4.8 kHz
 3 μ Hz for 4.8 kHz .. 3 μ Hz

Absolute frequency accuracy
 10^{-4} of selected frequency

Output voltages for ZGS, ZG4, ZG2 or G22 test interfaces

Ac voltage amplitude

0 .. 3 V (rms) below 10 MHz
 0 .. 2 V (rms) above 4 MHz for **ZG4** and **G22**
 0 .. 1 V (rms) above 10 MHz

Ac voltage resolution

0.7 mV from 3 V .. 100 mV
 6 μ V below 100 mV

Ac voltage accuracy

$\pm(10^{-2} + 10^{-2}/\text{MHz})$ of selected voltage $\pm 20 \mu\text{V}$

Ac voltage distortion

$2 \cdot 10^{-3}$ of selected voltage below 100 kHz at 1V rms

Dc bias voltage range with **ZGS, ZG4, ZG2 or G22 test interfaces and option B**

$\pm 40\text{V}$

Dc bias voltage resolution

10 mV

Dc bias voltage accuracy

$\pm 50 \text{ mV}$

Dc bias current limit

about $\pm 70 \text{ mA}$

Output impedance (ac and dc bias)

50 Ω

ZGS, ZG4 or ZG2 test interface current to voltage converter

Frequency range

3 μ Hz .. 20 MHz

Current ranges (rms)

40 mA, 15 mA, 1.5 mA, 150 μ A, 15 μ A, 1.5 μ A,
 150 nA, 15 nA, 1.5 nA, 150 pA, 15 pA, 1.5 pA

Current resolution (reproducibility)

$\pm 5 \text{ fA} \pm 10^{-5}$ of current range
 $\pm 30 \text{ fA/Hz} \cdot \text{frequency of measurement}$

Capacity range

$10^{-15} - 1 \text{ F}$

Resistance range

0.01 - $2 \cdot 10^{14} \Omega$

Accuracy in $\tan(\delta)$ for capacitive samples:

$\pm 3 \cdot 10^{-5} \pm 10^{-3}$ of measured value
for frequency between 10 Hz .. 100 kHz and
sample capacity between 50 pF .. 2 nF

For more detailed impedance measurement ranges and accuracy limits refer to the
"Measurement Ranges and Accuracy, Accuracy of Impedance Measurement" chapter.

ZGS, ZG4 or ZG2 test interface reference capacitors

63 build in low loss precision reference capacitors from 25 pF .. 2 nF

ZG4 interface differential voltage inputs V+, V-**Common mode rejection**

> 80 db below 100 kHz

> 60 db below 1 MHz

Input bias current

$< 2 \cdot 10^{-12} \text{ A}$

Input impedance

$> 10^{-12} \Omega$ in parallel $< 10 \text{ pF}$